Superconductor Electronics Monitor 2026

Markets, money, maturity, technology comparison

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2026

What you will find in this Monitor

A market and technology view of superconductor electronics (SCE) — digital logic, memory and mixed-signal built from Josephson junctions, whose largest branch is SFQ (Single Flux Quantum): where money is being made and invested today, how the contestable market develops to 2035, and the technological maturity that gates it. Every figure carries a source, a date, and a confidence tier.

HOW TO READ THE NUMBERS

T1	Demonstrated — primary peer-reviewed / datasheet source
T2	Corroborated — multiple independents tracing to a primary
T3	Vendor claim — single-source, not reproduced
T4	Modeled estimate — our scenario; assumptions stated
SRL	SCE-Readiness Level — a 1–9 judgment per subsystem, TRL-analogous, assigned by Qodeh on the demonstrations behind it; never blended across subsystems (p. 12)

SECTIONS

Every figure on these slides carries its confidence tier; sources are cited per slide and compiled, grouped, in the References (p. 17). What changed since v1.0: p. 32.

The primer

What is SFQ? Superconducting digital electronics built from Josephson junctions — the fastest, lowest-energy logic ever demonstrated

T1

$\Phi_0 = h/2e = 2.067\,833\,848 \times 10^{-15}$ Wb

The bit is Φ_0 — one flux quantum (or ½, or 2, by family): a constant of nature, identical in every device, immune to drift.

T1

~1 ps

Josephson-junction switching — logic demonstrated to 770 GHz (1999), still the fastest digital gate ever clocked in any technology

T1/T4

~10^{-19} J

energy per switch (ERSFQ) — ~1,000× below CMOS before the cryogenic tax, a conditional 10–30× after it

The Landauer frontier: adiabatic AQFP is measured at ~35× kT·ln2 at GHz speeds (a 21,460-JJ CPU exists); sub-Landauer switching remains reversible-and-simulated only — it costs ~10^3× in density and pays off first in qubit control, not CPUs. [T1 device / T4 system]

HOW IT COMPUTES

- Bits are single quanta of magnetic flux stored in superconducting loops; Josephson junctions switch in ~1 ps, emitting identical picosecond pulses instead of holding voltage levels
- Zero-resistance wiring carries those pulses ballistically — interconnect energy, the dominant cost in CMOS, nearly vanishes
- Circuits run at 4 kelvin in niobium and NbTiN foundry processes at 50–350 nm — 1990s-scale lithography at an exotic operating point
- 22 families in the 2026 roadmap register, in three token classes: flux-pulse (the SFQ core), flux-state (AQFP, RQFP) and non-flux (nanowire cryotrons, QPSJ). The field is SCE; "SFQ" names its largest branch.

WHAT IT IS NOT (the honest limits)

- Not dense: ~10^3–10^4× behind CMOS per mm²; the largest 4 K RAM ever demonstrated is 64 kb (2013 — a hybrid Josephson–CMOS part; pure-JJ record 4 kbit) — memory is the field's hardest gate
- Not room-temperature: every watt removed at 4.2 K costs ~230–7,000 W at the wall — the cryogenic tax, priced into every figure here
- Not mainstream: a handful of foundries, and no system-level design flow anyone can buy — ecosystem, not physics, sets today's pace

Sources: Chen & Likharev 1999 (770 GHz) · Mukhanov 2011 (ERSFQ) · Cryomech PT415 (cryogenic tax) / plant-FOM data. *Full references: p. 17.*

The primer

The highest speed, the asymptotically lowest energy, and the symbiosis with quantum computing secure a growing long-term future for SCE

CONTROLLING QUANTUM COMPUTERS

The near market driven by QC

- Superconducting-qubit machines hit a wiring wall: room-temperature control tops out near ~10^3 lines per cryostat — 10^5–10^6-qubit machines need electronics inside the fridge (Google control team, 2019; ETH budget analysis, 2019)
- SFQ is the only logic family that has demonstrated qubit-control waveform synthesis at millikelvin — up to 99.9% single-qubit fidelity (two-chip stack, Nature Electronics 2026) — independently replicated at 10 mK (SIMIT/CAS + Tokyo Univ. of Science + RIKEN, 2026) and again at 15 mK on a monolithic driver (NICT + Tohoku, EPJ QT, Jul 2026)
- IBM is exploring SFQ control with SEEQC under DARPA's QBI (2025); Japan's Moonshot funds SFQ qubit control & readout as a named theme

Contested by cryo-CMOS at 3–4 K (2–23 mW/qubit demonstrated) — this Monitor tracks both.

ENERGY-FRONTIER COMPUTING

The large, distant prize

- Projected 0.025 J/TFLOP wall-plug for a superconducting AI system incl. cooling — ~18× below Blackwell-class like-for-like (imec; projection, not silicon)
- Gated by memory (the 64 kb record) and by finding an accelerator model that fits SFQ's strengths

The bull case lives or dies here — see Market development (p. 9).

THz-CLASS ELECTRONICS

The top-speed edge

- Holds the outright digital speed record — a 770 GHz SFQ flip-flop (1999), unbeaten in any technology; complex circuits run at upper tens of GHz today (junction limit ~1 THz, fc ≈ 870 GHz)
- Fielded for over a decade in defense digital-RF receivers; a natural readout for superconducting single-photon-detector arrays

Small markets today — but the capability is unique and shipping.

Sources: Krinner et al., EPJ QT (2019); Bardin et al., JSSC (2019); Underwood et al., PRX Quantum (2024); SEEQC, Nature Electronics (2026); DARPA QBI (Jun 2025); JST Moonshot Goal 6; imec (2024). Full references: p. 17.

Twenty-two families, one pattern: everything that beats the bias wall is unbuilt

DC-BIASED bias sums across the die — ~10^4 devices/A

- ■ 25k **RSFQ** richest libraries + EDA; largest demonstrated logic circuit
  ✕ bias resistors burn static power; bias current caps the die
- ■ 4.9k **LR / LV-RSFQ** 30× less static power, no new physics
  ✕ still dc-biased; LR costs inductor area, LV costs margin
- ■ 6.8k **ERSFQ** zero static power; best control-plane ceiling (59k qubits)
  ✕ large bias inductors; worst devices/A in the block (9.5×10^3)
- ■ 2.6k **eSFQ** zero static, 2× devices/A, simpler bias tree
  ✕ every gate must be clocked — restricted cell set
- ■ 600 **Self-timed** no clock network — kills the top complexity limiter
  ✕ handshake JJs per gate; 600 switches is the whole record
- ■ 23 **DSFQ-LV** asynchronous; escapes path-balancing DFF explosion
  ✕ dynamic state decays — data must keep moving
- □ **TSFQ** timing-encoded: more per wire, unmodified RSFQ hardware
  ✕ resolution = jitter budget; needs precise delay lines
- □ **xSFQ** clockless dual-rail with return-to-zero built in
  ✕ 2 pulses/bit and dual-rail wiring — 2× the cost of a bit
- ■ 16 **HFQ / HFQ-LV** half energy AND half the L·Ic pin; best dc devices/A
  ✕ needs π-junctions (SRL 3–4) and half the noise margin

AC-POWERED waveform power, often the clock — >10^8/A

- ■ 809k **SFQ-AC** largest circuit ever fabricated in any family
  ✕ register class, not logic — no published clock rate
- ■ 73k **RQL** zero static, transformer-coupled, CMOS-EDA flow
  ✕ 4-phase AC clock distribution; 2 pulses/bit; one vendor
- □ **PML** phase state, not pulse event — immune to pulse loss
  ✕ nothing demonstrated; patents concentrated in one estate
- □ **PCL** fan-out without amplification; the JSRAM system story
  ✕ five years, zero measured logic gates; adds capacitors to the stack
- ■ 21k **AQFP** lowest measured switching energy (~1.4 zJ ≈ 35 kT·ln2)
  ✕ adiabatic ⇒ slow (MANA CPU ran at 100 kHz) and ~10^3× area
- ■ 28 **RQFP** logically reversible — the only route below Landauer
  ✕ 28 devices; 12 years of claims, no measured sub-Landauer

NEW 2026 & NON-FLUX two newcomers, two junction-free devices

- □ **FPL** inductorless: π phase batteries replace storage inductors (~100× density)
  ✕ wants a new NbTiN/AlN process; key table cells still '?'
- □ **SSBF** ballistic fluxons on a passive J+L path; energy recycled
  ✕ needs near-lossless lines; synchronisation undefined; nothing built
- ■ 32 **nTron / hTron** no junctions, single-layer fab; >10^9/A, drives warm electronics
  ✕ thermal switching ⇒ ns-class speed and reset; dissipative
- ■ 2 **QPSJ** charge dual (2e): zero static, immune to flux trapping
  ✕ 2 devices ever; ultra-disordered films; no logic family built

■ largest demonstrated circuit (switching devices) □ nothing demonstrated ✕ the cost gold = new to the IRDS roadmap in 2026

Read it as one sentence: the families that beat the bias wall (>10^8/A) pay in maturity — every one is □ or near it — while everything with a real circuit behind it is stuck near 10^4 devices per ampere. IRDS's own line: ***"Some logic families look attractive, but no substantial circuits have been demonstrated." Token classes: FPL and SSBF are flux-pulse families — the 2026 entrants — and only nTron/hTron and QPSJ carry no flux token.***

Table: "Superconductor Digital Logic Families" — IRDS CEQIP 2026 Update preview, Table CEQIP-4 (ISRDS Granada, May 2026) · 2023 IRDS CEQIP Tables workbook · the "cost" line under each family is this Monitor's synthesis from the table's own columns and the published record · T2 preview-grade.

The Monitor in eight numbers

A stronghold in superfast and millikelvin computing, with a path to HPC acceleration — the money is still small, soft and early

T4

$4–9B

contestable market, 2035 (computed $4.3–8.8B; bear $0.5–1.5B · base $3–8B · bull $20–35B)

T2

≈$140M

stated cumulative into SCE-first startups (SEEQC $80.8M per SEC) — vs $12.6B into quantum startups in 2025 alone: early, tiny, pre-inflection

T1

$1.8B

IonQ's completed acquisition of SkyWater (closed 31 Jul 2026) — the first SCE-capable fab now inside a quantum vendor

T4

$0.1–0.3B

today’s SCE-linked annual revenue base: defense digital-RF, metrology, QC-control co-development

770 GHz

fastest digital logic ever demonstrated — RSFQ, 1999

2.6 Mb/cm²

the densest functional superconducting memory ever demonstrated has no Josephson junctions in it — a 16-bit nanowire array (2026). The 4 K RAM record is still 64 kb (2013, hybrid J–CMOS); pure-JJ 4 kbit (1995). Memory gates general-purpose SCE.

×230–7,000

the cryogenic tax: ~1000× raw energy edge becomes a conditional 10–30×

~nW/qubit

projected ERSFQ control vs 2–23 mW/qubit demonstrated cryo-CMOS — why revenue starts in quantum

Sources: Chen & Likharev (1999); Van Duzer et al. (2013); cryogenics per Cryomech/NIST specs; Bardin (2019) & Underwood (2024); company filings & disclosures; McKinsey QTM 2026 (context); T4 = Qodeh scenarios, assumptions stated (p. 9). Full references: p. 17.

Where SCE earns money today: three lines — two of them quantum computing

GATE-MODEL QC: CONTROL & READOUT

The physics-favored segment

• SEEQC: only shipping mK-SFQ control hardware — QC controlled by SFQ digital electronics at millikelvin (Nature Electronics, 2026)

• NVIDIA NVQLink QPU–GPU digital link (2025); digital QEC interface with UK NQCC (2025)

• Customer-funded co-development: BASF, Merck lineage (QuPharma)

CO-DEVELOPMENT → EARLY PRODUCT

DEFENSE DIGITAL-RF

The quiet installed base

• Superconductor direct-RF receivers fielded for over a decade (Hypres lineage): 20–30 GHz sampling ADCs, ~75 dB SINAD class

• Renewed ADC demonstrations published 2025

• Opaque, defense-funded; ~low hundreds of $M with metrology & SQUIDs combined

NICHE PRODUCT (SUSTAINED)

ANNEALING QC: DACs AT SCALE

Also quantum computing — and the manufacturability proof

• Annealing is QC: D-Wave ships chips of more than a million JJ since 2020 (vendor statement) — on-chip SFQ/QFP DACs program every annealer (the largest demonstrated logic circuit is far smaller: ≈25k switches, RSFQ)

• The largest superconducting ICs in production anywhere

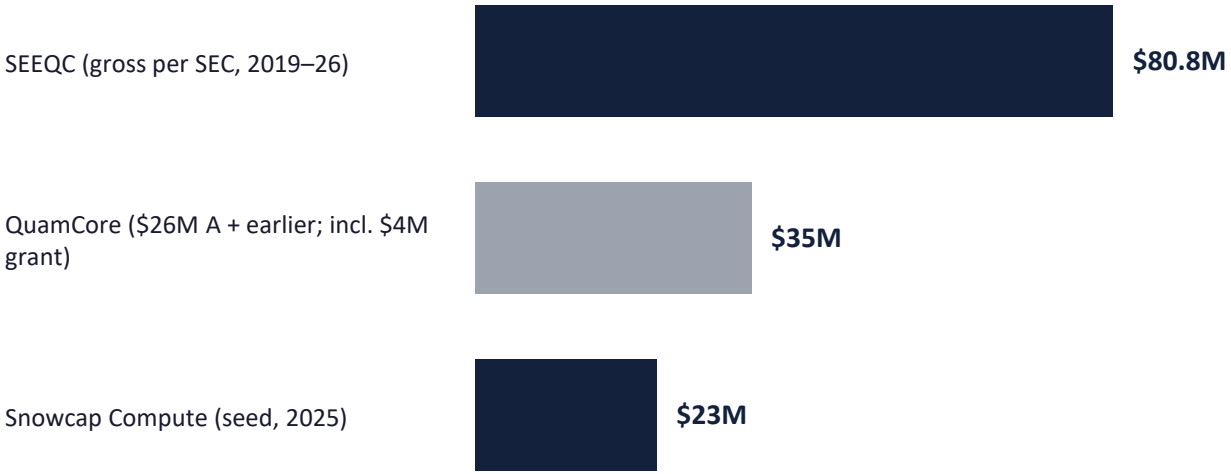
• Proves 10^6-JJ manufacturability the AI/HPC thesis depends on

IN PRODUCTION (ADJACENT)

Full references: p. 17.

SCE-first venture layer

Disclosed equity into SCE-first companies, $M — an upper bound on SCE-directed venture money



Three ledgers, read differently: (1) Venture — ≈$140M stated cumulative into SCE-first companies (SEEQC $80.8M gross per SEC, superseding the $52.4M aggregator figure): an upper bound on SCE-directed money (these companies also fund qubits, foundry services, and full systems; pure-play floor: Snowcap's $23M); ≈0.6% of 2025 quantum equity (the three 2025 rounds). (2) Corporate/M&A — the $1.8B SkyWater acquisition moved the only SFQ production fab inside a quantum vendor; the SFQ-attributable share of the price is not derivable. (3) State, the majority — mostly undisclosed; disclosed anchors: CAS RMB 1B (~$145M) initiative, NSF DISCoVER $15.0M Expedition, a DOE Accelerate share; order $150–400M/yr [T4]. The venture ledger — three disclosed companies worldwide — is the smallest and the most information-rich: its near-emptiness is itself evidence, and inflections announce themselves there first.

THE STRUCTURAL EVENT

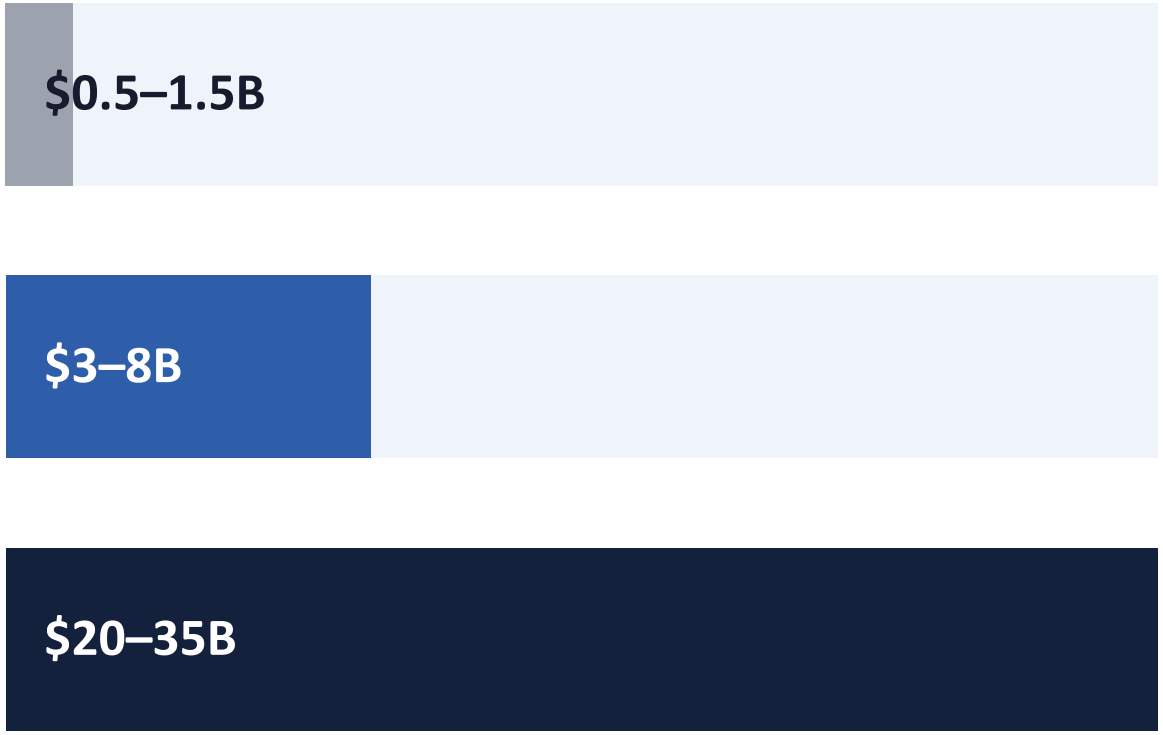
$1.8B

IonQ → SkyWater ($15.00 cash + 0.4883 IonQ shares per share): announced Jan 2026, shareholder-approved May 2026, closed 31 Jul 2026 — SkyWater operates as a subsidiary under its own name, with a general foundry-continuity pledge; Category-1A Trusted Foundry status was asserted at close, and post-close re-accreditation of the new entity is unconfirmed. The first SCE-capable Trusted Foundry now inside a vertically integrated quantum vendor — superconducting-program-specific continuity (e.g., the QuamCore co-development) remains the open question. The SFQ-attributable share of the price is not derivable: SkyWater does not disclose its SCE revenue.

New (Jun–Jul 2026): SEEQC's Allegro SPAC route was terminated on 25 Aug 2026 ("abandon the Transaction"), leaving a contingent $2M + $6M stock obligation to Allegro on any future IPO, acquisition or $100M raise; SEEQC's own S-1, filed 29 Jun 2026 while the SPAC was still pending, was amended on 28 Aug — the first SCE pure-play approaches the public markets on its own registration [T1, filings]. **Program signal:** still no dedicated US superconducting-digital program since IARPA C3 — though its toolchain lives on under NSF DISCoVER — though the May-2026 IBM / US-Commerce "Anderon" 300-mm quantum foundry ($1B CHIPS + $1B IBM, proposed; no definitive documents) names supporting-electronics wafers, superconducting wiring and TSVs in scope.

Sources: TechCrunch (Jan 2025); BusinessWire (Jun 2025); Ctech (Aug 2025, T2) + inferred pre-A (T3); IonQ/SkyWater filings; CAS: China Daily (2018); NSF award #2124453; McKinsey QTM 2026. *Full references: p. 17.*

Three market-size scenarios to 2035



Memory stays unsolved; imec-class milestones slip; QC scaling slips. SCE = QC control + defense RF niche.

QC control scales with 10^5-qubit machines; first cryo-AI inference pods deployed ~2030–32.

Rack-level 10–30× J/FLOP proven ~2030; energy-constrained AI buildout adopts cryo-pods (3–5% of accelerators).

Scenario-weighted mean ≈ $6.5B (endpoint band $4.3–8.8B): the mode is bear, yet the mean lands in upper-base — ~2/3 of it rides the 15% bull branch. Anchors — four different denominators: semiconductors $796B in 2025 → WSTS Spring-2026 forecast $1.51T in 2026 (+90%, memory ~250%) and ~$1.9T in 2027, so the denominator is moving faster than anything else in this model · AI accelerators $373B by 2030 → >$600B by 2033 (system-level; not a WSTS subset) · QC $43–71B by 2035 (all modalities; SCE rides the superconducting share) · datacenter electricity 945 TWh/yr (~0.95 PWh) by 2030. SCE contests value in fixed-infrastructure markets, never volume.

Source: Qodeh scenarios (T4, drivers stated); WSTS 2025 actual + Spring-2026 forecast; MarketsandMarkets 2025; McKinsey QTM 2026; IEA, Energy & AI 2025. A cryostat excludes mobile/client/edge — ~75% of logic demand. *Full references: p. 17.*

Four markets: when each turns on and what gates it

QC control & the QC→HPC interface

$0.5–2B by early 2030s

The only logic synthesizing control at mK; cryo-CMOS contests at 3–4 K. Photonic links (~3 pW/line), mK-CMOS mux (200 pW). Revenue now; scales with every 10^5-qubit program.

Gate: qubit-count scale-up itself

AI / HPC acceleration

$0 – $35B by 2035

Entirely scenario-dependent: wall-plug J/FLOP edge is ~18× on paper (BF16 vs B200), unproven in silicon.

Gates in order: memory (binary unlock) → system proof → miniaturization & 3D (throttle: sets whether share is 1% or 5%)

Defense digital-RF

$0.3–1B

Fielded niche with decades of heritage; grows with SIGINT/radar modernization; opaque budgets.

Gate: program-of-record wins

Metrology & other

~$0.1B

Josephson voltage standards, SQUID-adjacent; mature, stable, small.

Gate: none — steady state

Source: Qodeh scenario decomposition (all T4); gate evidence per References (p. 17). QC-control estimate = share of QC systems capex crossing to in-fridge digital control.

SCE value is stable, hard to disrupt, and set to grow

RATE

×10

SCE: most families run at 50–100 GHz. CMOS CPUs: 5.5–6.2 GHz; simpler CMOS logic reaches ~10 GHz.

Demonstrated [T1/T2]. *Junction physics allows ~870 GHz; what stands between 50 GHz and that is clock distribution and path balancing, not device speed.*

SYSTEM POWER

10–30×

Energy per operation for a whole system, after cooling. Raw device edge ≈1,000× (an ERSFQ switch dissipates ~2×10^{-19} J). Removing 1 W at 4.2 K costs 230–7,000 W at the wall — that tax is what turns 1,000× into 10–30×.

Projected [T4]. *No SCE system has ever computed a TFLOP, so the net figure has never been measured end to end.*

GATE POWER

nW vs mW

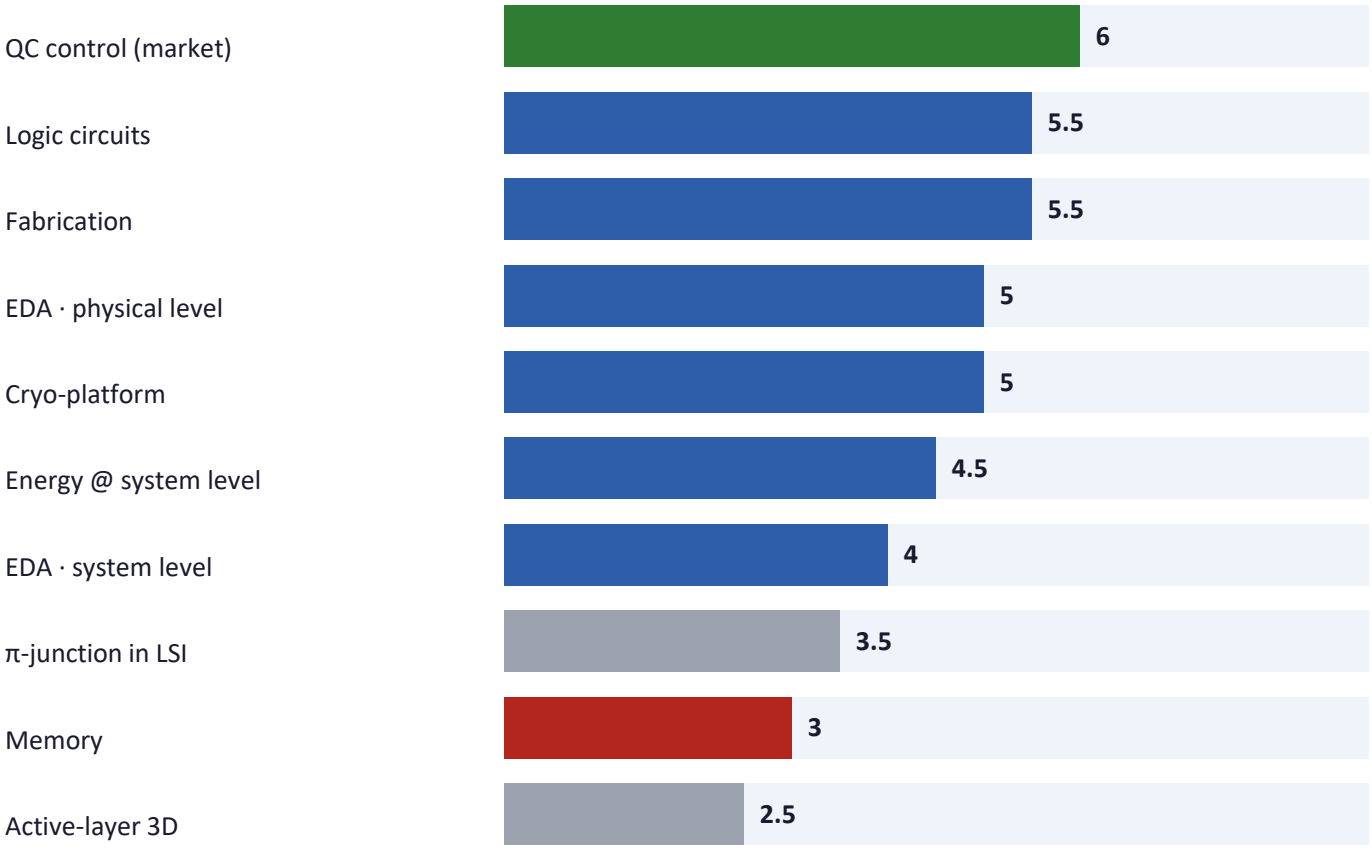
The only electronics that works in the millikelvin domain. SCE: ~1 nW/qubit — an ERSFQ projection. Cryo-CMOS: 2–23 mW/qubit — demonstrated at 3–4 K (Google 2019, IBM 2024).

Unsettled [T4]. Our own SCE estimates span ~1 nW to ~50 µW per qubit, so the ratio could be ~40× or ~10^7×. And the two figures are budgeted at different fridge stages: millikelvin, where total cooling capacity is microwatts, against 3–4 K, where it is watts.

Sources: PRBS-7 at 64.77 GHz RSFQ and 45.72 GHz ERSFQ (Inamdar et al., IEEE TASC 2023); switching energy Herr et al. (2011, 2013); cryogenic tax from large-plant and Cryomech PT415 specifications; CPU clocks from vendor datasheets; cryo-CMOS per-qubit power Bardin et al. (2019), Underwood et al. (2024); Full references: p. 17.

Readiness is wildly uneven — one subsystem blocks the money, one sets the ceiling, one sets the pace

SCE-Readiness Level (SRL, 1–9) by subsystem — never blended



BLOCKER · CEILING · CATALYST

Memory (SRL 3) — the blocker. The 4 K RAM record is 64 kb (2013, hybrid Josephson–CMOS; pure-JJ 4 kbit, 1995). The largest thing the field has built out of junctions is a shift register — 202,280 bits at exactly 4 JJ/bit, ≈0.32 Mb/cm²; the densest, a 72-bit RAM array at 0.88 Mb/cm² (2019). Both sit below a junction-free nanowire array. The AI/HPC-acceleration case on p. 10 rests on an unbuilt part: imec's JSRAM, 4 MB/cm² projected, no fabricated array 3.5 years on.

Density — the ceiling, and it is permanent. SCE sits $\times 2 \times 10^4$ behind CMOS as demonstrated (12,600 JJ/mm² in the payload of the 809k-JJ chip against N3E's ~216M transistors/mm²), $\times 10^3$ at process level, $\times 10^2$ on imec's projection. $L \cdot I_c \approx \Phi_o$ pins every storage loop, so flux logic ceilings at $\sim 10^7$–10^8 devices/cm². Only 3D active-layer stacking goes past that — SRL 2.5, no demo.

EDA (5 physical / 4 system) — the catalyst, and it is fragile. Extraction, LVS, DRC, flux-trapping validation and PDK compilation are a licensed product line — from SUN Magnetics, one supplier of fewer than ten people, which is why the field score is 5 and not the products' own 7–8. Above RTL there is nothing to buy: two academic flows exist, neither publicly distributed. None of this blocks the physics; it gates industrial acceptance.

SRL = SCE-Readiness Level: a TRL-analogous 1–9 judgment per subsystem, assigned by Qodeh from the demonstrations referenced on p. 17 — the scale is a judgment, the basis is T1.

Density: where the ceiling is, what raises it, and which market needs it raised

THE GAP TO CMOS

×2×10⁴

as demonstrated — 12,600 JJ/mm² in the payload of MIT-LL's 809k-JJ chip (2017; 4,340 chip-level on the 2025 108.5k part) against N3E's ~216M transistors/mm² [T1]

×10³

at best process capability — 1.3×10⁷ JJ/cm² on MIT-LL SC2, the 150-nm node [T1]

×10²

if imec delivers — 4M JJ/mm² in its 2024 design paper; no logic silicon exists on the platform yet [T3]

10⁷–10⁸ /cm²

the physics ceiling for ac-powered flux logic at ~100-nm wires — our derivation from Tolpygo's "a few million AQFPs per cm²" (2022): three to four orders below CMOS, and permanent

THE LEVERS — AND WHO HAS THEM

SRL 5 — **Kinetic inductors** MoN_x at 2–8 pH/□, NbTiN: storage loops ~10× smaller with the physics unchanged.
MIT-LL ● · imec ● · MIT.nano ● (NbN)

SRL 5–6 — **Self-shunted high-Jc junctions** No external shunt resistor, so a smaller cell; 80-nm junctions projected at NIST for Jc = 10 mA/μm² (fabricated: 1.5–2.7 μm at ≤3 mA/μm²).
MIT-LL ● · NIST ● · imec ● · VTT ● · SkyWater ● (recipe-owned)

SRL 3–4 — **π-junction phase batteries** A built-in π phase replaces the storage inductor: the $L \cdot Ic \approx \Phi_0$ constraint is removed, not shrunk.
Nagoya ● (Nb/PdNi/Nb on a 4-layer Nb process, 2025) · NICT ● (NbN/CuNi/NbN) · MIT-LL ▽ (PSE2 — node withdrawn)

SRL 2–3 — **Active-layer 3D** Stacking at μW/mm², which CMOS at ~1 W/mm² cannot do; the only lever that goes past the ceiling.
TSV: MIT-LL ● · VTT ● (offered) · QuantWare ◐ (VIO vertical interconnect; TSV undisclosed) — both qubit lines · imec – Stacked active logic: no one, anywhere

The two levers that reach furthest have the lowest readiness — and the integration technology sits in fabs that build qubits, not logic.

WHICH MARKET NEEDS IT RAISED

Defense digital-RF · metrology
Today's density suffices. Fielded for a decade; density is not on their critical path.

QC control (SRL 6)
Enters at today's density — revenue now. Scale-up does not: IRDS's 2026 preview puts ~7.5×10⁶ JJ of control per machine by 2032 and ~5×10⁸ at the 2038 handoff — ×10 and ×600 the largest digital IC ever fabricated (809k JJ).

AI / HPC acceleration
Needs the gap closed to ×10²–10³ and 3D on top of it — the two lowest-readiness levers. This is the market where density is the barrier.

Memory (SRL 3)
Needs every lever at once. The largest all-junction memory ever built is a shift register (≈0.32 Mb/cm²) and the densest a 72-bit RAM array (0.88 Mb/cm², 2019); the array that beats both has no junctions in it.

SRL per lever is Qodeh's judgment on the scale of p. 12 · ● fabricated and measured · ▽ withdrawn · – not found (searched). Sources: Tolpygo et al., IEEE TASC 2015/2019, arXiv:2210.02632; Semenov et al., arXiv:2501.03343; NIST, APL 122 (2023); imec IEDM 2024, arXiv:2411.08645; Fujimaki et al., IEICE E108.C (2025); IRDS CEQIP 2026 preview. Full references: p. 17.

Players by layer

FABS & PLATFORMS

- MIT Lincoln Lab — SFQ5ee / SFQ5hs / SFQ7ee, the research standard (task-order access)
- imec — 300-mm CMOS-compatible NbTiN platform (IEDM 2024)
- SEEQC foundry (ex-Hypres) · AIST QuFab — the one tariff-purchasable line · SIMIT (CN) — fabricates external designs; US Entity List 2024
- SkyWater — Trusted Foundry (re-accreditation post-close unconfirmed); IonQ subsidiary since 31 Jul 2026
- FLUXONICS (IPHT Jena) — European MPW, RSFQ1 rules; no arm’s-length customer run documented
- Nine fabs have ever made SCE logic — one contested; four take an outside design today; one publishes a price (p. 15)

PRODUCT & VENTURE

- SEEQC — mK-SFQ control; $80.8M gross per SEC; S-1 filed (Nasdaq: SEQC); NVIDIA/NVQLink
- Snowcap Compute — SFQ-for-AI; $23M seed (Jun 2025)
- QuamCore — clockless mK SFQ, stacked-chip (patent-documented); $35M reported
- D-Wave — 10^6-JJ chips in production · Hypres — digital-RF
- Northrop Grumman — RQL (publishes patents, not papers — 14 filings 2024–26)
- SUN Magnetics — the field's only commercial EDA supplier: InductEx, InductEx-LVS, TetraHenry, JoSIM-Pro; licensed since 2017; fewer than ten people

PROGRAMS & RESEARCH

- No US mission-agency SCE program since IARPA C3 — but the toolchain it built lives on (NSF DISCoVER)
- Japan: ¥130B quantum supplement (2025); AIST ¥100B
- Yokohama/Nagoya — AQFP, ALUs, π-junctions
- Rochester (Friedman) — design canon · MIT — nanowire memory
- Wisconsin/NIST — SFQ qubit control · Stellenbosch (Fourie) — InductEx and the ColdFlux tool lineage · USC / NSF DISCoVER — qPALACE v2 and SuperFlow, the system-level flows
- NICT + Tohoku — monolithic mK SFQ qubit driver, the third independent party (EPJ QT, Jul 2026)

Source: company/press disclosures 2024–26 (References, p. 17; T1–T3 by item). Fab and company columns: complete as publicly disclosed at cut-off; research poles: selected. Names are public facts, not endorsements.

Who makes what: each fab, what it has made, what its process can do

		WHAT THE FAB HAS MADE — logic families and memory, fabricated and measured								WHAT ITS PROCESS CAN DO — the density levers of p. 13, plus multilayer and bump					
Fab (click for profile)	**Access**	**RSFQ**	**ERSFQ / eSFQ**	**RQL**	**HFQ**	**SFQ-AC**	**AQFP**	**PCL / PML**	**Memory**	**π-junction**	**High-Jc / self-shunted**	**Kinetic L**	**Multilayer**	**TSV**	**Bump / flip-chip**
Fabs that have made superconductor digital logic — nine, one contested															
MIT-LL	G	● 2015–25	–	◐ NGC's	–	● 108.5k	● 2024	–	● VT RAM	● ▽ PSE2	●	● MoN_x	●	● 2020–23	● In
AIST QuFab	$	● 1KP 13/17	–	–	◐ Nagoya's	–	● 21k	–	–	–	–	–	● 9-lyr	● tooling	● tooling
SIMIT / SELF	X	● 32-bit	○	–	–	–	–	–	–	–	–	–	● 7-lyr	–	–
NIST Boulder	J	● 2017	–	–	–	–	–	–	–	○	● 3.0	–	● 4-lyr	–	● 2,193
Leibniz-IPHT	R	● RSFQ1H	–	–	–	–	● 2025	–	– none	–	–	–	● 3 Nb/14 mk	–	–
SEEQC foundry	Q	● 2026	○	–	–	–	–	–	–	·	·	·	● 4–8 Nb	·	·
NICT	J	● 2026	–	–	● NbN	–	–	–	–	● CuNi	·	·	·	·	·
NEC	J	◐ 2024	–	–	–	–	–	–	–	·	·	·	● 4 Nb	·	·
SkyWater / D-Wave recipe	C	○ QuamCore	–	◐ NGC's	–	–	–	–	–	–	● recipe	–	● 6+	–	·
Platforms and capability fabs — no logic made															
imec	J	–	–	–	–	○ design	–	○ design	○ JSRAM	–	● >2.5	● NbTiN	● 2-lvl	–	–
Nagoya University	J	–	–	–	–	–	–	–	● SR 2016	● PdNi	·	·	·	·	·
MIT.nano	U	–	–	–	–	–	–	–	● 2.6 Mb/cm²	–	–	● NbN	–	–	–
VTT (qubits)	Q	–	–	–	–	–	–	–	–	–	●	–	·	● offered	●
QuantWare (qubits)	Q	–	–	–	–	–	–	–	–	–	●	–	·	◐ VIO	●

Read it as: one row per fab — what it has made on the left, what its process can do on the right. RSFQ is the only family with more than four fabricators; AQFP has three; RQL has never had a line of its own, and Northrop is almost certainly fabless. PCL, PML, FPL, SSBF, DSFQ, xSFQ, self-timed SFQ and QPSJ have never been fabricated anywhere: the roadmap's twenty-two families are six in silicon. The capabilities scaled SCE needs sit in fabs that make no logic — π-junctions in two Japanese joint-research fabs, TSV and bump in qubit fabs — while imec has no TSV in any of its fourteen ASC 2026 items. For an outsider with a design and no insider there are four routes: tariff (AIST), quote (SEEQC), demand-triggered run (IPHT), negotiated contract (SkyWater). Each fab's name opens its profile (pp. 18–31).

● fabricated and measured, dated · ◐ made for a customer, or attribution incomplete / contested · ○ designed or announced only · ▽ withdrawn · – searched, not found · "·" not assessed. Access: $ published tariff · Q quote · R demand-triggered run · C negotiated contract · G government instrument only · J joint research only · U user programme (you bring the process) · X Entity-listed. High-Jc cells give Jc in mA/μm². Qodeh survey, September 2026: 31 organisations examined, one dossier per fab, every cell dated and sourced; T1 unless marked. Full references: p. 17.

The events that move the scenario weights

WOULD MOVE THE NUMBERS UP

- The first two-qubit entangling gate driven by SFQ or RQL pulses — zero experiments worldwide; the highest-information event on this list and the gate on the QC-control thesis
- imec's first 300-mm logic silicon — IEDM 2025 gave process advances only; of its fourteen ASC 2026 entries (eleven imec-led) the two nearest a circuit are titled “Design of…” and “Modeling…”
- A fabricated JSRAM macro — validates the entire SCE-AI roadmap; still a projection 3.5 years after the design paper
- Any 4 K RAM beyond 64 kb — resets a 13-year record
- FIRED — mK SFQ control is a field, not two programmes: NICT + Tohoku (EPJ QT, 9 Jul 2026) joins SEEQC and SIMIT/CAS + Tokyo Univ. of Science + RIKEN, probably a fourth in Shenzhen — all single-qubit only
- The first licensable system-level RTL→GDS flow — from an EDA house, from the physical-layer vendor, or by licensing qPALACE out; the tooling gap is commercial, not technical
- QuamCore test-vehicle silicon in the Nov 2026 – May 2027 window implied by the 12–18-month milestone language (SkyWater, 6 Nov 2025) — the first mK-native SFQ fabric
- Snowcap tapeout or architecture disclosure — and whether its fab and PCL licence get named
- SEEQC IPO pricing — its S-1 was filed 29 Jun 2026 with the SPAC still pending; the SPAC was terminated 25 Aug and the S-1 amended 28 Aug; the first SCE pure-play now approaches the market on its own registration
- A new major government or defense superconducting-digital programme — watch “Anderon” reaching definitive documents (nothing signed, no executive named since the May-2026 announcement) and SUPREME's 2027 PDKs
- π-junction phase-battery circuits at ≥10^3 JJ on foundry Nb — a cell-size lever for RSFQ and AQFP alike

WOULD MOVE THE NUMBERS DOWN

- IonQ–SkyWater integration: continuity pledged at close, but the FTC's behavioural order failed of adoption on an equally divided Commission — nothing binds the new owner to keep serving rivals. First checkpoint: IonQ investor day, 8 Sep 2026
- The SkyWater documentary window is already shut — Form 15 filed 10 Aug 2026; observability now runs through D-Wave's and IonQ's filings
- imec platform slip — metric: no ≥10^3-JJ clocked logic on 300 mm and no fabricated JSRAM array by end-2027
- Cryo-CMOS full control at ≤10 µW/qubit — the 4 K-budget line at 10^5 qubits; the nearest published anchor is a spin-qubit charge-readout IC at 18.5 µW/qubit (ISSCC 2025), a different modality
- Photonic links and mK multiplexing maturing — fibre ~3 pW/line vs ~14 nW for 0.085” stainless-steel coax; imec's 200 pW mK mux. Every control line they replace weakens the wiring-wall premise
- Superconducting design automation resting on soft-funded academic flows — qPALACE (ColdFlux lineage; v2 reported under NSF DISCoVER) and SuperFlow (NSF Expedition + JST FOREST, AQFP-only); neither is publicly distributed and neither carries a maintenance commitment. The most likely quiet failure in the tooling layer
- A quantum funding winter — freezes the QC-control bridge; defense RF becomes the floor
- Flux-trapping or yield surprises at >10^6 JJ integration

Items map to the scenario drivers (p. 9), the market gates (p. 10), or the funding ledgers (p. 8). Watch venues: ASC 2026 (Sep 6–11, Pittsburgh) — eleven imec-led items (fourteen with co-authored) · IEDM 2026 (12–16 Dec, San Francisco) · IEDM 2027 (4–8 Dec) · ISS (Japan, annual).

Published sources behind this Monitor

PEER-REVIEWED LITERATURE & PREPRINTS

Foundations & records: Likharev & Semenov, IEEE TAS 1 (1991) · Chen et al., IEEE TAS 9 (1999) · Mukhanov, IEEE TAS 21 (2011) · Herr et al., JAP 109 (2011) · Herr et al., JAP 113 (2013) · Takeuchi et al., APL 102 (2013) · APL 114 (2019) · Sci. Rep. 4 (2014) · Sci. Rep. 7 (2017) · npj QI 10 (2024) · Ayala et al., IEEE JSSC 56 (2021) · Van Duzer et al., IEEE TASC 23 (2013)

Fabrication & scaling: Tolpygo et al., IEEE TAS 25 (2015) · IEEE TAS 29 (2019) · Golden et al., arXiv:2501.03343 (2025) · Tolpygo et al., arXiv:2411.04045 (2024) · imec: IEDM 2024 · IEDM 2025 · IITC 2026 · Kundu et al. (imec), arXiv:2411.08645 (2024) · Herr et al., APL 122 (2023) · Medeiros et al., Nature Electronics 9 (2026) · Krylov, Jabbari & Friedman, Springer (2024)

Quantum control & decode: Liu et al., arXiv:2604.05693 (2026) · Lecocq et al., Nature 591 (2021) · Fallik et al., arXiv:2603.16608 (2026) · Krinner et al., EPJ QT 6:2 (2019) · Bardin et al., IEEE JSSC 54 (2019) · Underwood et al., PRX Quantum 5 (2024) · Acharya et al., Nature Electronics 6 (2023) · McDermott & Vavilov, PR Applied 2 (2014) · McDermott et al., QST 3 (2018) · Leonard et al., PR Applied 11 (2019) · Liu et al., PRX Quantum 4 (2023) · SEEQC et al., Nature Electronics 9 (2026) · Google Quantum AI, Nature 638 (2025) · Ueno et al., DAC (2021) · HPCA (2022) · Holmes et al., ISCA (2020)

DATASHEETS & TECHNICAL SPECIFICATIONS

NVIDIA H100 · NVIDIA B200 / Blackwell · Cryomech PT415 (Bluefors) · Bluefors XLD/XLDsl · Oxford Instruments Proteox · MIT Lincoln Laboratory foundry · FLUXONICS RSFQ1H rules · SUN Magnetics product line — InductEx, InductEx-LVS, TetraHenry, JoSIM-Pro (paid licence tiers since 2017) · SEEQC foundry process menu · HYPRES #S45/100/200 design rules Rev. 10 · CMOS node data (ISSCC 2025 / IEEE Spectrum)

COMPANY FILINGS & DISCLOSURES

QuamCore PCT WO2025243306A2 · Northrop US9652571B2 (RTL→GDSII) · D-Wave (QBTS) 10-K FY2025 · SkyWater (SKYT) 10-K FY2025 · IonQ–SkyWater close (31 Jul 2026) · SEEQC registration statement (28 Aug 2026) & Allegro SPAC termination (25 Aug 2026) · FTC Matter 2610061 (behavioural order failed of adoption) · SkyWater Form 15-12G (10 Aug 2026) · SEEQC $30M (TechCrunch, Jan 2025) · SEEQC Series A (BusinessWire, 2020) · Snowcap Compute launch (Jun 2025) · QuamCore Series A (Ctech, Aug 2025) · NVIDIA NVQLink (Oct 2025) · SkyWater–QuamCore (Nov 2025) · D-Wave Advantage2 GA (May 2025)

GOVERNMENT & PROGRAM DOCUMENTS

AIST QuFab (tariff foundry service) · IARPA C3 · IARPA SuperTools · DARPA QBI — IBM × SEEQC (Jun 2025) · JST Moonshot Goal 6 · US DOE “Accelerate” (Sep 2023) · NSA Superconducting Technology Assessment (2005) · NSF DISCoVER Expedition — D. S. Holmes, “DISCoVER Expedition Status (qPALACE v2),” ISEC 2025 · AIST QuFab price list & terms of use (2026) · METI superconducting-foundry review (Jul 2026) · EU Chips-JU / NanoIC (2026)

MARKET CONTEXT

McKinsey Quantum Technology Monitor (2026) · WSTS (2025 actual; Spring-2026 forecast, Jun 2026) · MarketsandMarkets accelerator forecast (2025) · IEA, Energy & AI (2025) · Europractice MPW prices (2026)

← Who makes what, p. 15

MIT Lincoln Laboratory

government research / prototyping foundry (USAF FFRDC), captive to USG sponsors — not a merchant foundry [T1 facts; T4 label]

Not a merchant foundry; its public menu understates the line (SFQ5ee+, SMCM4m, In bumps appear only in outside papers) and it is the fab of record for Northrop's RQL; '2025 NbN self-shunted process' is junction work, not a released node.

IDENTITY & CONTROL

Location Lexington / Hanscom AFB, Massachusetts, USA — Microelectronics Laboratory (MEL) inside the Microsystems Prototyping Foundry; 200 mm wafers, 90 nm-class tooling [T1]

Ownership MIT-operated Dept of War (ex-DoD) FFRDC sponsored by the USAF; cost-reimbursement, no fee. No change of control; contract vehicle changed 2025-04-01: FA8702-15-D-0001 → FA8702-25-D-B002 (to 2035; ~US$12.2 bn ceiling [T2]) [T1]

Strategy Gives the USG a domestic, trusted, high-yield SCE IC source while advancing the node itself; sponsor task orders, no product revenue. SFQ digital family and the SQUILL qubit foundry share the fab but have separate access models [T1]

Funding USAF FFRDC primes FA8702-15-D-0001 (2015–25) and FA8702-25-D-B002 (2025–35), no fee [T1]; LPS seeded SQUILL 2021, multiyear 2023 [T1]; IARPA C3/cryogenic computing widely associated, no contract number found [T3]

ACCESS & PROCESS

Access USG-mediated: USAF FFRDC task order (non-DoW via IAA); industry via CRADA/SBIR-STTR; academia via collaboration; tariff, MPW, PDK NOT FOUND. Latest outside silicon: Yokohama Natl Univ AQFP, run SFQ5A9, 2024-11-06, co-authored [T1]

Processes SFQ5ee 350 nm, 100 μA/μm², 8 Nb + MoNx kinetic inductor, Nb/Al-AlOx/Nb JJ; SFQ5hs 200 μA/μm²; SFQ5ee+ 9 Nb, 250 nm (2024); SFQ7ee 10-layer with self-shunted NbN/NbNx/NbN JJs in development (2025-12); PSE2 SIS + SFS π-junctions (2019) [T1]

Capacity NOT FOUND — runs/yr, wafer starts, turnaround unpublished; only indirect: SQUILL 400+ devices to 30+ groups (2023-07-05); run codes like SFQ5A9 imply a modest lettered run series [T4]

Withdrawn SFQ3ee/SFQ4ee legacy, absent from current page [T1 by absence]; SFQ6ee unused after 2020 and PSE2 absent from current menu — superseded/lapsed inferred [T4]; no MIT-LL statement of any technology being dropped

WHAT IT HAS MADE — dated, measured

- AC-biased SFQ shift registers, 108,500 JJ per 5×5 mm chip, ~1 defect per million JJs, with Stony Brook — 2025-01-06 [T1]
- AQFP cells and 69-stage AQFP shift registers in SFQ5ee+ (run SFQ5A9), with Yokohama National University — 2024-11-06 [T1]
- ELASIC 88×88 mm superconducting IC in SFQ5ee, reticles interconnected without stitching — 2023-07-21 [T1]
- Northrop Grumman RQL: 72,800-JJ yield vehicles (2015) and 5×5 mm RQL chips in SFQ5ee with SMCM4m MCM carrier + In bumps (2021-04-28) [T1]
- Self-shunted NbN/NbNx/NbN JJs on 200 mm, Jc ~10 μA/μm² to ~1 mA/μm², IcRn ≈0.5 mV (SFQ7ee enabler) — 2025-12 [T1]

Open *SC1 / SC2 are process-development nodes from the literature, not menu items; MPW cadence, tariff, NDA terms, ITAR/EAR statement and memory arrays: NOT FOUND · Under what instrument were Yokohama National University's designs fabricated? Co-authorship is the only visible external path for SFQ digital · SFQ5ee minimum junction 700 nm vs 500 nm in different sources; SFQ7ee schedule unresolved*

Profile compiled from public sources and dated to 2025-12; tiers as marked; NOT FOUND = searched and not found. One of fourteen fab profiles; the matrix on p. 15 is their summary. Full references: p. 17.

← Who makes what, p. 15

AIST QuFab

government open shuttle / multi-project foundry (AIST ORP shared facility) with a published per-tool-hour tariff [T1]

Japan's most open SFQ/AQFP foundry — a foreign company has bought silicon [T1 METI] — but the 1KP RSFQ library is incomplete, 8-inch exists only in METI's roadmap, and an end-2026 business-structure decision could change access.

IDENTITY & CONTROL

Location AIST Tsukuba Central, Japan — federation of cleanrooms (CR1–CR9 etc.), 720 m², mainly Class 1000; 100 mm (4-inch) wafers; METI roadmap 8-inch 2026–27, 12-inch early 2030s [T1]

Ownership AIST (R&D agency under METI); run by G-QuAT's Quantum Device Research Team; ex-CRAVITY, rebranded Qufab 2024 (foundry service 2024-10). METI: foundry business structure to be decided by end-2026 [T1]; private operation reported [T3]

Strategy Shared prototyping facility for quantum computers/annealers and qubit-control circuits (Nb SFQ/AQFP, Al-JJ qubit, 3-D packaging sub-lines); cost-recovery tool-time billing, not wafer pricing; Japan's de facto Nb-SFQ pilot line [T1/T2]

Funding AIST ORP cost-recovery scheme + ARIM terms; JST Moonshot JPMJFR212B (2022–28) and JSPS JP19H05614/JP19H05615 on the 2024 qubit-control work [T1]; Qufab-specific NEDO/MEXT grant or 2025 quantum-supplement line item NOT FOUND

ACCESS & PROCESS

Access Open-call shuttle (2-monthly rounds), overseas eligible; export-control and 'national competitiveness' screens; overseas ×2 tool rate + 50% admin; run price on request. Foreign silicon: USC + TOBB SFQ ADC on HSTP, 2025-10, arm's-length [T1]

Processes PHSTP: 4 Nb, 10 kA/cm², 2.4 Ω/□, 7.1×7.1 mm, 1.0 µm; 1KP (new FY2026): 4 Nb, 1 kA/cm², 1.2 Ω/□, 5×5 mm; both Nb/Al-AlOx/Nb; HSTP FY2025 only. 9/11-layer interconnect advertised but not on the shuttle menu [T1]

Capacity 12 shuttle runs planned FY2026 (6 PHSTP + 6 1KP) [T1]; ¥320 m cumulative revenue over 312 cases since 2024-10 (~¥1 m/case) [T1 METI]; 16 external users (12 academic, 4 firms), 3 overseas; turnaround, wafer starts NOT FOUND

Withdrawn HSTP absent from FY2026 menu (PHSTP absorbed its 7.1×7.1 mm reticle) [T1]; CRAVITY-era STP2/ADP2 absent from FY2025/26 calls [T1 absence; T4 'discontinued']; CRAVITY website 404 (2026-09-03); item Qufab045 gone from price list

WHAT IT HAS MADE — dated, measured

- RSFQ 17-cell library on 1KP: 13 cells correct at 100 kHz, margins >60% (AND, NOR, TFF, T1FF failed) — 2025-11-21 [T1]
- AQFP buffer chain, AND, XOR and full adder on 1KP operated correctly at 100 kHz — 2025-11-21 [T1]
- SFQ ADC with digital-SQUID modulator + TFF counter on HSTP, USC + TOBB, tested in the authors' own cryocooler — 2025-10 [T1]
- AQFP-mux qubit-control circuit for >1,000 qubits via one cable, with YNU/Tohoku/NEC, on AIST's superconducting IC process — 2024-06-03 [T1]
- MANA 4-bit AQFP microprocessor, 21,460 JJ, 1.4 zJ/op — YNU design on the AIST Nb process — 2020-12 [T2]

Open *Who are the 3 overseas users (2 academic, 1 company)? METI counts them, names none; AIST's achievements page is still 'in preparation' · Does the end-2026 business-structure decision preserve open/overseas access? Is the METI 8-inch (2026–27) step real — AIST itself is silent · Shuttle wafer/chip price, design rules, turnaround, yield, JJ density: NOT FOUND; π-junction/magnetic, NbTiN, kinetic-inductor modules NOT FOUND*

Profile compiled from public sources and dated to 2026-09-01; tiers as marked; NOT FOUND = searched and not found. One of fourteen fab profiles; the matrix on p. 15 is their summary. Full references: p. 17.

← Who makes what, p. 15

SIMIT / SELF (CAS)

institute-owned dedicated R&D / pilot process platform (150 nm class), not a merchant foundry; US Entity-Listed [T2]

Nb04 (7 Nb, 15 kA/cm²), the ICT-CAS 32-bit processor (2024-06-01) and the Entity Listing are all confirmed — but the listing is quantum-justified, the RMB 1 bn programme names ICT-CAS not SIMIT, and 'JSICcompiler' is unverified.

IDENTITY & CONTROL

Location Shanghai, China (Changning and Jiading sites per BIS listing) — Superconducting Electronics Facility (SELF); 100 mm (4-inch) wafers for the Nb digital process, platform described as 4/6-inch [T1/T2]

Ownership CAS institute (ex-Shanghai Institute of Metallurgy), no corporate parent; hosts the Shanghai Key Lab of Superconducting IC Technology. US BIS Entity List effective 2024-05-09 (89 FR 41886, presumption of denial, quantum justification) [T1]

Strategy Domestic superconducting IC process for SFQ logic, SNSPDs, SQUIDs and qubit control; state-grant funded, no wafer revenue; fab partner in the ICT-CAS-led CAS RMB 1 bn superconducting-computer programme [T2/T4]; SNSPDs industrialised [T2]

Funding CAS Strategic Priority XDA18000000, XDB0670000; National Key R&D 2021YFB0300400; NSFC 62171437, 92164101, 92576207; Shanghai S&T 21DZ1101000, 25LZ2600600; Guangdong 2020B0303030002 [T1]; RMB 1 bn programme names ICT-CAS, not SIMIT [T3]

ACCESS & PROCESS

Access Sanctioned (US Entity List); no open priced service — PDK pages unreachable (TLS); MPW, price list, terms NOT FOUND. Silicon to domestic partners (ICT-CAS, 2024-06-01) and a Japanese co-author (Tokyo Univ. of Science/RIKEN, 2026-04) [T1]

Processes SIMIT Nb03 (4 Nb layers, Jc NOT FOUND; IRDS-listed 2020); Nb03P (parameters NOT FOUND); Nb04: 7 Nb + Mo resistor (3 Ω/sq), 19 masks, 15 kA/cm², 0.5 µm min JJ, CMP, Nb/Al-AlOx/Nb on 100 mm (2023) [T1]; nothing beyond Nb04 found

Capacity NOT FOUND — no runs/yr, wafer starts, lot size or turnaround in any reachable source (EN + 中文); PDK pages unreachable, not absent

Withdrawn NOT FOUND — no discontinued node or technology reported; the 2018-projected 770 GHz CPU prototype 'as early as 2022' appears unmet but no cancellation is stated

WHAT IT HAS MADE — dated, measured

- Millikelvin SFQ qubit controller made at SELF: >99.9% avg Clifford fidelity, ~0.121 fJ/gate, 10 mK — 2026-04 (arXiv:2604.05693) [T1]
- 32-bit bit-parallel SFQ string-matching processor on SIMIT-Nb03P, 12 GHz, 251 GOPS/W, with ICT-CAS — 2024-06-01 [T1]
- RSFQ standard cells on Nb04 with −40%/+40% bias margins — 2023-04 (arXiv:2304.01588) [T1]
- SUSHI neuromorphic SFQ chip on SIMIT-Nb03: 2 neurons / 6,701 JJ measured (32-neuron / 99,982-JJ version simulated only) — 2023-10 [T2]
- 4-Nb-layer cell library for LSI superconductor digital circuits, all-SIMIT authorship — 2025-05 (IEEE TAS) [T1]

Open *Jc and layer count of Nb03/Nb03P unpublished; what 'P' means and how Nb03P (silicon 2024-06) relates chronologically to Nb04 (paper 2023-04) · Is there a 6-inch digital node, or is 6-inch confined to SNSPD? Capacity entirely unpublished; date of the State Key Lab renaming and CENSE founding unknown · 'JSICcompiler' RTL-to-GDSII flow NOT VERIFIED — only JSICsim (2022) and a ~2023 IEEE RTL-to-GDSII paper found; EU/Japan listings of SIMIT NOT FOUND*

Profile compiled from public sources and dated to 2026-04; tiers as marked; NOT FOUND = searched and not found. One of fourteen fab profiles; the matrix on p. 15 is their summary. Full references: p. 17.

← Who makes what, p. 15

NIST Boulder

government research / metrology-production hybrid line (Boulder Microfabrication Facility) with a published instrument tariff [T1 facts; T4 label]

The only logic-making line with a published tariff for superconducting silicon (PJVS chips) — and its self-shunted junctions were measured at 1.5–2.7 µm and up to 3 mA/µm²; the 80-nm figure is a projection at 10 mA/µm², not a fabricated device.

IDENTITY & CONTROL

Location NIST Boulder Laboratories, 325 Broadway, Boulder, Colorado, USA — BMF 1,700 m² ISO 5 cleanroom; SCE processes on 3-inch (76.2 mm) Si, coupons to 150 mm [T1]

Ownership NIST, US Department of Commerce; internal facility under the NIST Act, no contract vehicle; no change of control ever [T1]. SCE work split between CTL's Superconductive Electronics Group and PML, which manages the BMF

Strategy Two missions on one line: realise the volt and ship it as hardware (PJVS/JAWS sold via the SRI programme), plus SFQ/microwave circuits for qubit control and energy-efficient computing; captive for R&D, commercial for finished hardware [T1]

Funding NIST appropriations; National Quantum Initiative Act framework; DoD 'FSDL' programme (unexpanded, no number); collaborators DOE SQMS, Google, Menlo Micro; BIPM (2024-10), INTA (2023-12) and NMIs incl. CN, IN [T1]; contract numbers NOT FOUND

ACCESS & PROCESS

Access Published tariff: SRI 6000 PJVS US$30,300–344,400 + $3,000 calibration, chip-only SKUs, EXW (2026-04-27) [T1]; BMF: NIST staff and direct collaborators only; SFQ via co-authorship (PRX Quantum 2023); deliveries INTA 2023-12, BIPM 2024-10

Processes No node codes: planarized 4-Nb SFQ, self-shunted Nb/NbxSi1-x/Nb JJs 2.7 µm, 4.2 kA/cm², PdAu resistor (2019); 3-layer a-Si variant 1 kA/cm² (2023); Nb/a-Si/Nb JJs Jc 0.01–3 mA/µm², IcRn 0.8–1.56 mV (2023); PJVS >270k JJ [T1]

Capacity NOT FOUND — runs/yr, wafer starts, turnaround unpublished (delivery 'case-by-case'). Indirect: 1,700 m² ISO-5, 19 deposition / 14 etch tools, ~60% of NIST-Boulder research uses the BMF; instrument-volume output, no publishable figure [T4]

Withdrawn No product withdrawn from the SRI catalogue and no discontinuation statement [searched negative]; Nb–PdAu–Nb and Nb–MoSi2–Nb barriers of the early 2000s no longer described — retirement inferred [T4]

WHAT IT HAS MADE — dated, measured

- SFQ digital qubit control: dc-to-SFQ driver chips flip-chipped (~2,193 In bumps) to transmons, error per Clifford 1.2(1)% — PRX Quantum 4, 030310, 2023 [T1]
- Nb/a-Si/Nb high-Jc junctions, Jc up to 3 mA/µm², IcRn to 1.56 mV, measured JJ diameters 1.5–2.7 µm — APL 122, 182601, 2023-05 [T1]
- Planarized 4-Nb-layer SFQ process with self-shunted Nb/NbxSi1-x/Nb JJs on 3-inch wafers — IEEE TAS, 2019-02-18 [T1]
- RSFQ cells (JTL, SFQ↔DC converters, T and D flip-flops) tested at low speed through 26-GHz probes — ISEC 2017 [T1]
- PJVS >270,000 JJ/chip ±10 V and JAWS >100,000 JJ in serial production and sold — ongoing, page 2026-04-27 [T1]

Open *Is the 2019 4-Nb planarized SFQ process still current, or has the Nb/a-Si JJ been folded into a newer unnamed node? What is 'FSDL'? · BMF as open user facility — contradicted (staff and direct collaborators only; not CNST NanoFab); MPW, NDA terms, memory arrays, named logic families NOT FOUND · PJVS shipped to China and other non-allied NMIs — confirm export classification since the 2024-11 spec; 250k vs >270k JJ/chip discrepancy unresolved*

Profile compiled from public sources and dated to 2026-05-04; tiers as marked; NOT FOUND = searched and not found. One of fourteen fab profiles; the matrix on p. 15 is their summary. Full references: p. 17.

← Who makes what, p. 15

Leibniz-IPHT / FLUXONICS

research-institute Nb line with a small demand-triggered open foundry service (FLUXONICS e.V. brokers access, owns no cleanroom) [T1]

Real Nb line and Europe's only advertised open digital foundry, but frozen at 1990s-class geometry on RSFQ1H (1 kA/cm², 12.5 µm² JJs, 2017 rules), foundry page static since 2024-07-26, and no arm's-length customer ever identified.

IDENTITY & CONTROL

Location Jena, Thuringia, Germany — Competence Center for Micro- and Nanotechnologies (KMNT), ISO 4, 700 m²; 100 mm (4-inch) wafers (stated for CJ2) [T1]

Ownership Leibniz-IPHT e.V., Leibniz Association member, Bund/Länder funded; change of control NOT FOUND. Access broker FLUXONICS e.V. is chaired from IPHT — structural conflict noted [T1 fact; T4 reading]; export-control statement NOT FOUND

Strategy Supplies IPHT's own quantum-sensing research and serves as Europe's shared Nb Josephson foundry for academics and small industry via cost-sharing multi-customer wafers, up to small-series production; hybrid, leaning consortium [T1]

Funding Leibniz Bund/Länder base funding [T2]; 'EU, FLUXONICS e.V.' credited for the digital work, no grant numbers [T1]; named partner in the EU SUPREME quantum pilot line (€25 m EU / ~€50 m) [T1]; historic EU network instrument NOT FOUND

ACCESS & PROCESS

Access Demand-triggered: 'two wafer runs per year depending on customer requests'; public design rules + DRC; tariff, NDA terms, dated call NOT FOUND. Arm's-length outside silicon NOT FOUND — all results have IPHT/TU Ilmenau co-authors

Processes RSFQ1H (rules v1.6, 2017-03-10): 14 layers, 1 kA/cm² ±20%, min JJ 12.5 µm², 2.5 µm features, Mo 1 Ω/□; CJ2 (v1.1, 2023-11-21): 100 mm, 11-layer, Nb/Al/Nb cross-type JJ 600×600 nm, 1.7 kA/cm² (custom available), AuPd 3 Ω/□ [T1]

Capacity Two advertised runs/yr, conditional on demand, placement deadlines end-March/end-September [T1]; wafer starts, wafers/run, yield NOT FOUND; turnaround NOT FOUND — queue latency up to ~6 months inferable [T4]

Withdrawn NOT FOUND — no process formally discontinued; RSFQ1H rules unrevised since 2017-03-10 while CJ2 was revised 2023-11-21 — de facto stagnation inferred, not a discontinuation [T4]

WHAT IT HAS MADE — dated, measured

- AQFP designed and characterised using sub-µm cross-type JJ (CJ2) technology — 2025 (authors not exposed on the FLUXONICS page) [T1]
- CJ2 cross-type sub-µm Nb/AlOx/Nb process for mixed-signal circuits, IEEE TAS — 2024-01 (IPHT's own process paper) [T2]
- RSFQ cells on RSFQ1H; TU Ilmenau maintains a fabricated-and-tested 13-cell library — undated [T1/T2]
- SQUIDs/SQIFs: long-baseline LTS gradiometers with sub-µm JJs (2020), field-tolerant SQIF current sensors (2021); commercialised via Supracon [T1]
- SNSPDs and microwave-resonance / bias-line studies (2020) [T1/T2]

Open *Who authored the 2025 AQFP paper and was any co-author external? Best candidate for a real external result (DOI unfetched) · Did the two advertised runs actually occur in 2024–26? No run ever announced; is RSFQ1H still run at all, and on what wafer size? · Tariff, arm's-length user, memory, energy-efficient SFQ, π-junctions, TSV/flip-chip, NbN/NbTiN process, JJ density, grant numbers: NOT FOUND*

Profile compiled from public sources and dated to 2025-12-03; tiers as marked; NOT FOUND = searched and not found. One of fourteen fab profiles; the matrix on p. 15 is their summary. Full references: p. 17.

← Who makes what, p. 15

SEEQC foundry

commercial merchant foundry, small-volume / pilot scale (in-house line also serving its own SFQ qubit-control products) [T1/T3]

Route to market was a failed SPAC, not a clean S-1: Allegro merger terminated 2026-08-25, IPO filed 2026-08-28; the Hypres sublease-in-holdover claim is unconfirmed ('transfer of assets' is the only primary); no foundry customer named.

IDENTITY & CONTROL

Location 150 Clearbrook Road, Elmsford, New York, USA (HQ + in-house foundry); 150 mm wafers [T1/T3]; offices London and Naples; planned second line in Taiwan with ITRI (2025-12-01)

Ownership Independent private Delaware corp., 2019 Hypres spin-out by asset transfer [T1]; no change of control. Allegro SPAC merger terminated 2026-08-25; IPO registration 2026-08-28; owes Allegro up to $2 m + $6 m stock on a trigger event [T1]

Strategy Fabricates its own SFQ chips for qubit control and sells merchant Nb foundry services; ~95% of 2025 revenue from engineering/integration services, 5% product [T1]; foundry framed as supply-chain independence; no customer named

Funding M Ventures $5 m (2020-04); $22.4 m Series A led by EQT Ventures (2020-09-16); $30 m (2025-01-14) [T2/T3]; $65 m PIPE + $75 m offering never consummated [T1]; '$80.8 m since inception' UNVERIFIED; CHIPS/contract numbers NOT FOUND

ACCESS & PROCESS

Access Published process menu, MPW + dedicated wafers, quote-based; TAT 6/8 wks (4/6 layers) [T3]; MPW calendar, NDA terms, Trusted/ITAR status NOT FOUND. Outside silicon: FY2025 foundry revenue confirmed (2026-08-28), no counterparty dated [T1]

Processes 150 mm; Nb and NbNx; 4/5/6/8 layers; Jc 100 / 1,000 / 4,500 / 10,000 A/cm²; resistors Mo 1.0 & 2.1 Ω/□, PdAu 2.1, MoNx 4.0 Ω/□; PECVD SiO2 + low-loss SiNx [T3]; min JJ size, Ic spread, JJ density, 8-layer planarisation NOT FOUND

Capacity Turnaround 6 weeks (4 Nb) / 8 weeks (6 layers) — the only published SCE TAT in Group B [T3]; runs/yr, wafer starts, cleanroom area NOT FOUND; $3 m NY Empire State Development facility expansion is the only sizing datum [T3]

Withdrawn Jc 30 A/cm² and 20,000 A/cm² options of the inherited Hypres menu (Rev. 10, 2015-03-01) absent from SEEQC's published menu [T1/T3 fact; T4 reason]; Allegro SPAC route abandoned 2026-08-25 [T1]; retired fabrication technology NOT FOUND

WHAT IT HAS MADE — dated, measured

- SFQ digital control chip + 5-qubit processor at 10 mK, 1Q fidelity >99.5% (peak >99.9%), Nature Electronics — 2026-03-18 [T1]; fab of each chip not stated
- Multi-layer SFQ circuit fabrication as a standing in-house capability — SEC registration statement, 2026-08-28 [T1]
- Merchant fabrication (prototype fabrication, custom chip development, process optimisation) generating FY2025 revenue — 2026-08-28 [T1]

Open *Does SEEQC own or lease its cleanroom, and from whom? Sublease/holdover claim: circulating, no primary found · Who fabricated the chips in the 2026-03-18 Nature Electronics result? Not stated; the in-house line is inference [T4] · No named external foundry customer; no DMEA Trusted accreditation or ITAR/EAR statement found; ITRI Taiwan line wafer size/site/funding undisclosed*

Profile compiled from public sources and dated to 2026-08-28; tiers as marked; NOT FOUND = searched and not found. One of fourteen fab profiles; the matrix on p. 15 is their summary. Full references: p. 17.

← Who makes what, p. 15

NICT

government research line (nitride NbN/NbTiN/TiN/MgB2) with a shared-use component; joint research only, not a foundry [T1]

Japan's only nitride SCE line; it put an SFQ driver on-chip with a qubit without degrading T1 (2026-07-09) — but access is collaboration-only, no wafer size or process parameters published, and no foreign party has received NICT silicon.

IDENTITY & CONTROL

Location NICT Kobe, Nishi-ku, Kobe, Hyogo, Japan — Advanced ICT Device Lab Kobe (cleanroom 1996; Device Co-creation Building 2024-03); wafer diameter NOT FOUND [T1]

Ownership NICT, national R&D agency under the Ministry of Internal Affairs and Communications (not METI/MEXT) [T2]; no change of control; Device Co-creation Building opened 2024-03; the long-standing NbN process lead is now deputy, not lab head [T1]

Strategy Not a foundry: NbN/TiN instead of Nb for higher temperature — SNSPDs for quantum comms, SFQ qubit-interface circuits, MgB2 diagnostics; devices for own programmes and collaborators; facility open to researchers at home and abroad [T1]

Funding JSPS KAKENHI JP19H05615, JP18H05211 (2026); JST PRESTO JPMJPR1669/JPMJPR2106, CREST JPMJCR1775, ERATO JPMJER1601/JPMJER2402; MEXT Q-LEAP JPMXS0118068682; JST ALCA, AMED [T1]; QIH FY2025 supplement ¥3.35 bn [T2]; Moonshot/NEDO NOT FOUND

ACCESS & PROCESS

Access Joint research only; tariff, cadence, screening, export clause NOT FOUND. Latest: SNSPDs to Tohoku Univ 2025-09-24; SFQ-driver/flux-qubit chip with Nagoya/Tohoku/AIST 2026-07-09 — domestic, co-authored; foreign recipient NOT FOUND [T1]

Processes No node menu. Epitaxial NbN/AlN/NbN JJs (few-μA Ic); TiN(200)-buffered NbN tri-layers on Si(100), JJ 1–40 μm; NbN/CuNi/NbN π-junction; NbN SNSPD process; NbTiN, MgB2 also on the line. Layers, Jc, min feature, wafer size NOT FOUND [T1]

Capacity NOT FOUND — runs/yr, wafer starts, turnaround, prices, cleanroom class/area all unpublished; only ~1,941 users (internal + external) in FY2018 across the whole Device Lab [T1]

Withdrawn NOT FOUND — no node menu or price list against which withdrawal could be detected and no discontinuation statement; emphasis has shifted from detector physics toward qubit-interface integration [T4]

WHAT IT HAS MADE — dated, measured

- NbN SFQ driver monolithically integrated with a flux-bias-free flux qubit; T1 undegraded vs microwave control — EPJ Quantum Technology, 2026-07-09 [T1]
- Superconducting photon detectors fabricated and supplied for a Tohoku Univ. entangled-photon router (1.3% loss, 99.3% switching) — 2025-09-24 [T1]
- NbN-based half-flux-quantum (HFQ) element for integration with superconducting qubits — APL, 2024-04 [T2]
- Wide-strip SNSPD with high-critical-current bank structure — Optica Quantum 1(1), 2023 [T1]
- NbN/CuNi/NbN π phase shifter on Si: half-flux-quantum shift in SQUID modulation — Sci. Rep., 2020-08-13 [T1]

Open *Can an external party buy NbN fabrication at Kobe, or only obtain devices in-kind through joint research? The key access question · Wafer size, layer count, Jc, yield of the NbN/AlN/NbN line NOT FOUND — no like-for-like comparison with AIST; capacity to scale the 2026 result unknown · Two national π-junction routes (Nagoya Nb/PdNi/Nb vs NICT NbN/CuNi/NbN) — any convergence or industrialisation? NICT's part in the 64-qubit machine not itemised*

Profile compiled from public sources and dated to 2026-07-09; tiers as marked; NOT FOUND = searched and not found. One of fourteen fab profiles; the matrix on p. 15 is their summary. Full references: p. 17.

← Who makes what, p. 15

NEC

captive corporate R&D process (low-power SFQ qubit-control circuitry), not a foundry, no external access [T1/T4]

NEC owns a real 250 A/cm² SFQ process — Japan's lowest Jc, 4× below AIST's 1KP — on no foundry menu; METI (2026-07-08) names AIST Qufab as Japan's only shared foundry, so NEC's line is captive by the government's own account.

IDENTITY & CONTROL

Location NEC research laboratories, Japan (Secure System Platform Research Laboratories); specific site NOT FOUND; wafer diameter NOT FOUND

Ownership NEC Corporation, private company [T1]. NEC authors carried joint NEC + AIST affiliations in the 2023 paper and were NEC-only by 2024-12 — a visible unwinding or re-scoping of an NEC–AIST joint arrangement [T1 fact; T4 interpretation]

Strategy SFQ-based digital control of qubits as a component play inside Japan's quantum-computer supply chain, not a computing-logic play; NEC named by JETRO in supply-chain roadmap work for large-scale quantum systems (2026-03-01) [T1/T2]

Funding NOT FOUND — no grant numbers retrievable from the abstracts obtained; JETRO-named participant in national quantum supply-chain roadmap work [T2]

ACCESS & PROCESS

Access NO access: tariff, application route, cadence, terms NOT FOUND; collaboration only. Latest external party: Nagoya University by co-authorship, 2024-12-24 (not arm's-length); foreign party and export-control statement NOT FOUND [T1]

Processes NEC 250 A/cm² process: four planarised Nb layers + Pd resistor layer; 2–10 µA JJs 'using conventional facilities'; 0.1–0.5 mV bias; ~1 nW/JJ; simulated 10 GHz [T1]. Junction size, JJ density, min feature, wafer size NOT FOUND

Capacity NOT FOUND — no capacity, throughput, turnaround or price [T1]

Withdrawn NOT FOUND — no roadmap, run schedule or statement of discontinuation; NEC publishes results, not a process datasheet [T1]

WHAT IT HAS MADE — dated, measured

- Low-power RSFQ cell library on 250 A/cm²: correct at 0.3 K, 8-bit shift registers to 8.5 GHz, power ~1/50–1/250 of conventional — IEEE TAS, 2024-12-24 [T1]
- Low-power SFQ circuits fabricated on the lowered-Jc process — IEEE TAS 2023-03-02; high-frequency operation reported at ICICDT 2023 [T1/T2]
- NEC co-authorship on the AIST/YNU AQFP-mux qubit controller, chip fabricated at AIST — 2024-06-03 [T1]
- Historical: NEC/ISTEC SFQ standard logic cell library (2002); first superconducting charge qubit (1999) [T2]

Open *Which physical line runs the 250 A/cm² process? 'Conventional facilities' + 2023 AIST cross-affiliations point at AIST Tsukuba, but no facility is named · Why did the NEC authors' AIST cross-affiliation disappear between 2023-03 and 2024-12 — end of a secondment, joint lab or programme? · Site, wafer size, cleanroom, junction size, JJ density, capacity, price, roadmap, grant numbers: all NOT FOUND*

Profile compiled from public sources and dated to 2026-03-01; tiers as marked; NOT FOUND = searched and not found. One of fourteen fab profiles; the matrix on p. 15 is their summary. Full references: p. 17.

← Who makes what, p. 15

SkyWater / D-Wave recipe

commercial merchant foundry (DMEA Category 1A Trusted Fab, 'Technology as a Service') running third-party superconducting recipes; D-Wave owns its recipe and buys line time [T1]

D-Wave's fab changed hands six weeks ago: IonQ, a competitor, now owns the line; the FTC's behavioural order failed of adoption on an equally divided Commission, so nothing binds it to serve the eight quantum customers. D-Wave's exact JJ count is unpublished — the vendor says 'more than 1 million'.

IDENTITY & CONTROL

Location 2401 East 86th Street, Bloomington, Minnesota, USA (ex-Cypress 8-inch line; 91,000 sq ft class 10); 200 mm wafers [T1/T3]; packaging site Kissimmee, Florida; 'SkyWater Texas' segment

Ownership SkyWater Foundry, Inc., wholly owned by IonQ since 2026-07-31 ($15.00 cash + 0.4883 IonQ shares/share, ~$1.8 bn [T3]); FTC Matter 2610061: Commission equally divided (1–1), behavioural order failed of adoption; Form 15-12G 2026-08-10 [T1]. D-Wave line agreement since 2012-12-23

Strategy Sells access to a US-owned Trusted 200 mm fab (TaaS); superconducting is one special-module franchise; eight quantum customers end-2025 [T1 FTC], Infineon 43% of FY2025 revenue [T1]. D-Wave: fab-lite, owns its recipe improvements [T1]

Funding DMEA Trusted Fab (MN; FL in process) [T1]; D-Wave line agreement, pricing redacted [T1]; QuamCore contract, amount undisclosed [T3]; CHIPS Act award, government contract numbers NOT FOUND; FY2025 revenue $442.1 m, quantum ATS +>30% [T1]

ACCESS & PROCESS

Access Bilateral contract only: D-Wave agreement (non-exclusive, 6 months' notice, price redacted) [T1]; QuamCore SFQ contract 2025-11-06 [T3]. Tariff, MPW, PDK NOT FOUND. Latest outside silicon: D-Wave Advantage2 qubits, 2025-03-12 [T1/T3]

Processes SC node, Jc, JJ size NOT FOUND. Own page: 200 mm, '6+ metal layers', 'JJ dep and etch', 'Nb damascene' [T3]. 'D-Wave six-metal-layer process' per Northrop (2021): 0.25 µm (5 layers), 0.5 µm top, Jc 10 µA/µm² [T1]; JJ material unpublished

Capacity SC-specific runs/yr, wafer starts, turnaround NOT FOUND; fab-wide ~10,000 30-mask CMOS wafers/month, 91,000 sq ft [T3]; D-Wave batches contractually 12–25 wafers, capacity bought as quarterly 'moves' [T1]

Withdrawn SC process withdrawn: NOT FOUND [T1]; SEC reporting discontinued (Form 25-NSE 2026-07-31, Form 15-12G 2026-08-10); independent existence ended 2026-07-31; D-Wave's 2007 JPL wafer fab superseded by this line, JPL now packaging only [T2/T4]

WHAT IT HAS MADE — dated, measured

- D-Wave Advantage2 annealing processor (4,400+ qubits) fabricated at the 200 mm Minnesota fab; beyond-classical result in Science — 2025-03-12 [T1/T3]
- Northrop Grumman RQL chips (10×10 mm) in 'the D-Wave six-metal layer process' for a multi-chip resonator clock network — 2021-04-28 (arXiv:2109.00560) [T1]
- D-Wave third-generation Φ-DAC on-chip flux-bias circuitry, 3× footprint reduction via fabrication-technology changes — 2021 (arXiv:2108.02322) [T1]
- Continuing production wafer relationship: 16th Amendment with a '2025 Spend Commitment' — effective 2025-02-21 [T1]
- D-Wave on-chip cryogenic control of a fluxonium qubit via a multilayer control chip, bump-bonded at NASA JPL — 2026-01-06 [T1]; wafer fab not stated

Open *Was DMEA Trusted accreditation re-granted after the 2026-07-31 change of control? No post-close notice found · Does merchant SC access survive IonQ ownership? Watch D-Wave's filings for a 17th amendment; the other seven quantum customers are unnamed · No SC process datasheet, MPW, tariff or PDK; the QuamCore cryo-SFQ test vehicle (window from ~Nov 2026) would be the line's first named SFQ digital silicon*

Profile compiled from public sources and dated to 2026-08-10; tiers as marked; NOT FOUND = searched and not found. One of fourteen fab profiles; the matrix on p. 15 is their summary. Full references: p. 17.

← Who makes what, p. 15

imec

captive research / R&D pilot-line platform in a 300 mm CMOS cleanroom — not a merchant foundry for SCE [T1/T4]

Upheld: every circulating imec circuit number is a projection — JSRAM '4 MB/cm²' is projected in its own source, the ASC 2026 shift register is 'Design of…', '50 nm' is interconnect linewidth (JJ CD 210 nm); no TSV shown.

IDENTITY & CONTROL

Location Kapeldreef 75, Leuven, Belgium — 300 mm CMOS pilot cleanroom; imec USA (Kissimmee, FL / NY) carries several superconducting authors [T1]; 300 mm wafers

Ownership imec vzw, independent Belgian non-profit (est. 1984); no change of control; new Chairman and CEO effective April 2026 [T1]; hosts NanoIC (€700 m CMOS) and leads SPINS (€50 m spin-qubit) pilot lines — neither is SCE [T1]

Strategy Platform R&D, not a service: CMOS-fab-compatible 300 mm superconducting digital tech for datacentre AI compute; affiliate + Flemish/EU funding, no named SCD grant [T4]. PCL/JSRAM originators left for Snowcap 2025-06-23 [T1/T2]

Funding SCD grant number NOT FOUND [T1 neg]; core funding Flemish Government + industrial affiliate programme [T2]; adjacent EU pilot lines NanoIC (€700 m sub-2 nm CMOS) and SPINS (€50 m spin qubits) are not SCE [T1]

ACCESS & PROCESS

Access NO purchasable service: tariff, MPW, PDK, NDA terms, export status NOT FOUND [T1 neg]. Only route is co-authored collaboration (ASC 2026 flux-trapping papers); no evidence any external party ever received imec superconducting silicon [T1]

Processes No named node. NbTiN/a-Si/NbTiN on 300 mm: interconnect 50 nm CD, Jc >120 mA/µm², Tc >13 K, 420 °C BEOL-compatible; JJ Jc >2.5 mA/µm², 210 nm CD; NbTiN/HZO MIM ~28 fF/µm² [T1]; 16 levels / 28 nm projected [T3/T4]; no resistor layer, no TSV

Capacity NOT FOUND on every measure — no runs/yr, wafer starts, turnaround or lot cadence for the superconducting platform; presumably internal R&D lots only [T4]

Withdrawn Nb-electrode JJs replaced by NbTiN electrodes with a-Si barrier [T1]; PCL/JSRAM absent from ASC 2026 titles after their originators left — shift inferred, no discontinuation stated [T4]; formally discontinued process NOT FOUND

WHAT IT HAS MADE — dated, measured

- NbTiN superconducting interconnects, 50 nm CD, Jc >120 mA/µm², Tc >13 K, two-level semi-damascene — IITC 2023 / IEDM 2024; press 2024-12-10 [T1]
- aSi/NbTiN Josephson junctions, Jc >2.5 mA/µm² ('record-high'), 210 nm critical dimension — IEDM 2024; imec article 2024-06-04 [T1]
- NbTiN/HZO/NbTiN MIM capacitors ~28 fF/µm² — IEDM 2024 [T1]
- Functional flux-trapping mitigation structures — IEDM 2025 paper 15-3, 2025-12-09 [T1]
- Adjacent: Al overlap-JJ transmons >100 µs, 99.94% 1Q fidelity — on coupons, NOT the 300 mm line — npj QI, 2022-10-17 [T1]

Open *Does ASC 2026 poster 4EPo1B (5ML resonator-powered shift register) contain measured data behind its 'Design of…' title? Re-check after 6–11 Sep 2026 · Did IEDM 2025 15-3 report a measured circuit or only components (paywalled)? Does PCL/JSRAM survive its originators' move to Snowcap, and where does it fab? · JJ density never published ('500×' is a baseline-less claim [T3]); 'PDKs in 2027' belongs to SUPREME, not imec; no SCD lead, partners or resistor layer*

Profile compiled from public sources and dated to 2026-09-06; tiers as marked; NOT FOUND = searched and not found. One of fourteen fab profiles; the matrix on p. 15 is their summary. Full references: p. 17.

← Who makes what, p. 15

Nagoya University

university research line — captive junction/thin-film process development (Nb, NbN, NbTiN, π/magnetic barriers); integrated circuits made on other lines (AIST, NICT) [T2/T4]

Small captive research junction line, not a foundry: the HFQ shift-register claim is confirmed (2025-06-01) but its fab is unnamed, and 'CONNECT library belongs to Nagoya' is NOT CONFIRMED — the 2010 library was YNU-led.

IDENTITY & CONTROL

Location Nagoya University (Higashiyama campus), Nagoya, Aichi, Japan — Graduate School of Engineering superconductor-electronics lab; wafer diameter NOT FOUND; own cleanroom vs shared nanofab unresolved

Ownership Nagoya University, Tokai National Higher Education and Research System → MEXT [T2]; facility-use agreement, tariff or application route NOT FOUND; no change of control; laboratory lineage continuous since 1993 [T1]

Strategy Develops device physics no foundry offers — π/magnetic junctions, NbN/NbTiN junctions for ~10 K, HFQ and gate-level-pipelined SFQ concepts; grant-funded (KAKENHI, JST), no fee-for-service; designs go to AIST's Nb and NICT's NbN lines [T4]

Funding JSPS KAKENHI JP19H05615, JP18H05211 (2026 paper); JP19H05614, JP18H01493; JST PRESTO JPMJPR1669, CREST JPMJCR1775, ERATO JPMJER1601; MEXT Q-LEAP JPMXS0118068682 (2020 paper) [T1]; Moonshot/NEDO/2025-supplement numbers NOT FOUND

ACCESS & PROCESS

Access NO — tariff, shuttle, cadence NOT FOUND; collaboration/co-authorship only [T1 absence]. External party receiving Nagoya devices NOT FOUND — Nagoya receives silicon (Nb 4-layer 10 kA/cm², AIST inferred [T4]; NICT NbN; NEC 250 A/cm²)

Processes In-house junction/film work 1993–2019: Nb/AlOx/Nb, all-NbN, NbTiN/Al-AlNx/NbTiN for ~10 K, NbTiN/Hf barrier, SFIS π-junctions (2017); Nb/PdNi/Nb π-junction 0-0-π SQUID on Nb 4-layer 10 kA/cm² [T1]; layers, Jc, density NOT FOUND

Capacity NOT FOUND — runs/yr, wafer starts, turnaround, prices all unpublished [T1 absence]

Withdrawn NOT FOUND — no price list or node menu to test; the NbTiN/Hf-barrier programme (2015–19) has no output after 2019 as focus moved to π/magnetic junctions, HFQ and qubit-interface circuits — priority shift, not a discontinuation [T4]

WHAT IT HAS MADE — dated, measured

- HFQ 4-bit shift register with 0-0-π SQUIDs (Nb/PdNi/Nb π-junctions) on Nb 4-layer 10 kA/cm²: 0.12–0.18 μW/bit, ~1/10 of SFQ — IEICE, 2025-06-01 [T1]
- Monolithic SFQ driver + flux-bias-free flux qubit on NICT epitaxial NbN/AlN/NbN, T1 undegraded (with NICT, AIST, Tohoku) — 2026-07-09 [T1]
- Low-power SFQ cell library on NEC's 250 A/cm² process: 8-bit shift registers to 8.5 GHz at 0.3 K — 2024-12-24 [T1]
- π-junction negative-inductance flux-transfer circuits — Supercond. Sci. Technol., 2024 [T2]; NbN HFQ element for qubit integration — APL, 2024-04 [T2]
- 48 GHz, 5.6 mW gate-level-pipelined SFQ multiplier — ISSCC 2019 [T2]; SFIS π-junctions with IC-grade Ic uniformity — APEX, 2017-02-13 [T1]

Open *Which fab ran the 2025 HFQ shift register? 'Nb 4-layer 10 kA/cm²' matches AIST HSTP/PHSTP (inference); PdNi π-junction an AIST layer or Nagoya post-process? · Own cleanroom or shared university nanofab? No facility page reachable; no wafer size, layer count, Jc or design rules for any Nagoya-owned process · Has the PdNi π-junction module yielded beyond 4 bits? No larger HFQ circuit found; the 'CONNECT' library name appears in no retrieved source*

Profile compiled from public sources and dated to 2026-07-09; tiers as marked; NOT FOUND = searched and not found. One of fourteen fab profiles; the matrix on p. 15 is their summary. Full references: p. 17.

← Who makes what, p. 15

MIT.nano (Berggren group)

open-access university shared cleanroom (Fab.nano) hosting a research group's junction-free NbN nanowire process — not a foundry, not a captive line [T2]

Densest addressable superconducting memory array published (16-bit, 2.6 Mbit/cm²) came from MIT's shared campus fab on a three-mask, junction-free NbN process — not Lincoln Laboratory, not a foundry; though fabricated there only 'in part'.

IDENTITY & CONTROL

Location MIT campus, Cambridge, Massachusetts, USA — MIT.nano, ~50,000 ft² cleanroom (ISO 5/6/7); memory process on 100 mm thermal-oxide wafers (facility wafer sizes unpublished) [T1/T2]

Ownership Owned and operated by MIT as a central facility — not a national lab, not government-operated; distinct from the MIT Lincoln Laboratory 200 mm line; no change of control; access via 'Become a user' programme and MIT.nano Consortium [T1/T2]

Strategy Shared-user research cleanroom for MIT and external users; the QNN group uses it for nanowire electronics (SNSPDs, nTron/hTron switches, memory) and ion-beam lithography; grant/philanthropy funded, no commercial revenue model [T1]

Funding US DOE Office of Science Microelectronics Codesign project LAB 212491 (primary support) [T1]; Breakthrough Starshot Foundation (initial memory concept) [T1]; NDSEG, NSF GRFP and MIT fellowships [T1]

ACCESS & PROCESS

Access Tool access only: third parties join as users/Consortium members; the QNN memory process is not offered. Rate card, MPW, NDA, export status NOT FOUND. Outside silicon NOT FOUND; only a Northeastern co-author (2026-01-06) [T1]

Processes NbN nanowire memory process: 100 mm thermal-oxide wafer, 23 nm NbN at 800 °C (Tc 12.5 K, 78 Ω/□, ~8.6 pH/□), three lithography levels (NbN, PECVD SiO2, Au enable lines), liftoff; NO Josephson junctions, Jc N/A [T1]; min linewidth NOT FOUND

Capacity NOT FOUND — runs/yr, wafer starts, turnaround, yield unpublished; a research process on a shared ~50,000 ft² facility, no throughput concept applies [T2/T4]

Withdrawn NOT FOUND — no discontinued process; the material portfolio has broadened (NbN → MgB2, MoSi, epitaxial NbN)

WHAT IT HAS MADE — dated, measured

- 4×4 (16-bit) row–column nanowire memory array: 2.6 Mbit/cm², BER 1e-5 at 1 MHz, 1.3 K, 46 fJ write / 31 fJ read — Nature Electronics 9, 69, 2026-01-06 [T1]
- Superconducting full-wave bridge rectifier (nanowire) — Nature Electronics 8, 417, 2025 [T1]
- nTron ripple counter integrated with an SNSPD on one chip — Phys. Rev. Appl. 22(2), 2024 [T1]
- hTron thermal switch SPICE-model extraction; photolithography-compatible three-terminal switch driving CMOS loads — Phys. Rev. Appl. 24(2), 2025 [T1]
- Wafer-scale MgB2 devices (ACS Nano, 2024); MoSi SNSPDs on LiNbO3 waveguides (ACS Photonics, 2024); optical coherent control of a qubit (Nat. Phys., 2025) [T1]

Open *Where was the 23 nm NbN grown? 800 °C deposition is not confirmed as a MIT.nano tool and the paper says 'in part' — top verification item · No MIT.nano rate card, wafer-size spec, MPW or export statement; opening year (2018) held at T4, unverified; no yield or minimum linewidth published · Scaling beyond 4×4 and merging with the photolithography-compatible switch process: no dated statement; 16 bits is an array demo, not a capacity*

Profile compiled from public sources and dated to 2026-01-06; tiers as marked; NOT FOUND = searched and not found. One of fourteen fab profiles; the matrix on p. 15 is their summary. Full references: p. 17.

← Who makes what, p. 15

VTT

state-owned research + pilot line with a commercial R&D / PDK-piloting / equipment-access service; SUPREME coordinator; quantum-oriented, not digital [T1/T4]

200 mm line with a commercial offer and the digital-capable ingredients imec lacks (trilayer JJs, TSV, flip-chip) — but none of it is applied to digital logic and no Jc, junction size or layer count is published; SUPREME PDKs due 2027.

IDENTITY & CONTROL

Location Micronova, Espoo, Finland — 2,600 m² ISO 4–6 cleanroom, 'largest R&D cleanroom in the Nordic countries'; 200 mm wafers, 300 mm planned 2026–2028 [T1]

Ownership Teknologian Tutkimuskeskus VTT Oy, non-profit company wholly owned by the Finnish State (corporatised 2015); no change of control; co-owns Finland's national quantum computers with IQM; spin-out SemiQon [T1/T2]; export statement NOT FOUND

Strategy Micro/nano R&D and piloting fab (MEMS, RF, photonics, quantum, superconducting); sells R&D services, PDK-based piloting and equipment access to start-ups through large firms; superconducting work driven by VTT+IQM and SUPREME [T1]

Funding Finnish state funding [T2]; Chips JU partner in FAMES, APECS, NanoIC (101183266/101183277), PIXEurope; SUPREME coordinator (€25 m EU / ~€50 m; grant number NOT FOUND); Chips Act projects fund 300 mm/TSV upgrades (numbers NOT FOUND) [T1]

ACCESS & PROCESS

Access Commercial offer (R&D, PDK piloting, cleanroom access) quoted on enquiry; tariff, MPW, public PDK, NDA terms NOT FOUND [T1 neg]. Arm's-length outside silicon NOT FOUND — VTT–IQM 50-qubit machine is a joint venture, SemiQon a spin-off [T1]

Processes No named node, Jc, junction size or layer count [T1 neg]. Named capabilities: trilayer Josephson junctions, Manhattan qubits, superconducting TSV and flip-chip, wafer bonding/3D integration; Cu TSV grinding 2026–28 [T1]

Capacity NOT FOUND — runs/yr, wafer starts, turnaround, yield unpublished; facility scale 2,600 m² ISO 4–6, 200 mm [T1]

Withdrawn NOT FOUND — nothing identified as dropped; trajectory expansionary (200 → 300 mm, added TSV capability) [T1 neg]

WHAT IT HAS MADE — dated, measured

- Transmon qubits: VTT+IQM 50-qubit quantum computer, 'first 50-qubit machine developed in Europe', operating — VTT news, undated [T2]
- Trilayer Josephson junctions and Manhattan-geometry junctions — named fabricated process capabilities, no parameters [T1]
- Superconducting TSV and flip-chip — named offered capabilities; no specific measured TSV result located [T1/T4]

Open *Parameters of the trilayer JJ process (Jc, size, layers) — nothing published; could VTT host digital SFQ in principle? · Is 'superconducting TSV' demonstrated and measured or only a capability statement? Do not report as demonstrated · Has any unaffiliated third party bought a VTT superconducting run? Will the 2026–28 300 mm upgrade cover superconducting processes? Kvanttinova scope unknown*

Profile compiled from public sources and dated to 2026-05-13; tiers as marked; NOT FOUND = searched and not found. One of fourteen fab profiles; the matrix on p. 15 is their summary. Full references: p. 17.

← Who makes what, p. 15

QuantWare

commercial merchant superconducting QPU supplier with a productised Foundry Service; owner-operator status of a cleanroom unconfirmed [T1/T4]

Nearest thing to a commercial European foundry, but not the 'commercial European Nb foundry': material never named, cleanroom ownership unconfirmed, no SFQ or memory, and no dated third-party foundry run since the 2022 launch.

IDENTITY & CONTROL

Location Molengraaffsingel 8, Delft, Netherlands (office suite on the TU Delft campus/science park); wafer diameter NOT FOUND; whether it operates its own fab NOT FOUND

Ownership QuantWare B.V., venture-backed ($178 m raised; investors NOT FOUND) [T3]; no change of control; SUPREME partner (2025-07), possible but unconfirmed Dutch fab site [T1]; export statement NOT FOUND despite shipping to 20 countries

Strategy Sells QPUs (A-Line, D-Line), Foundry Services and VIO 3D-interconnect packaging; core bet is VIO scaling to 10,000-qubit QPUs by 2028; 2026 Gold Edison Award claimed [T3]; Group C's only unambiguous merchant, quantum not digital [T1]

Funding $178 m raised cumulative (company-stated; investors NOT FOUND) [T3]; SUPREME partner (€25 m EU / ~€50 m first phase; grant number NOT FOUND) [T1]; no Dutch national programme identified; product revenue [T3]

ACCESS & PROCESS

Access Foundry Services (quote-based) for third-party qubit designs; tariff, MPW, PDK, NDA terms NOT FOUND [T1 neg]. Outside silicon: 'customers in 20 countries', 'largest commercial QPU supplier' [T3, aggregate]; dated third-party run NOT FOUND

Processes No node, wafer size, material, Jc, JJ size, layers or design rules [T1 neg]. Disclosed: >100 µs T1, JJ targeting/trimming, 'negligible kinetic inductance', VIO vertical interconnect; planar ≤176 I/O now; VIO-400 2026, 1K 2027, 40K 2028 [T3]

Capacity NOT FOUND on every conventional measure (runs, wafer starts, turnaround, yield); only vendor aggregates — 'shipped more quantum processors than any other commercial supplier' [T3]

Withdrawn NOT FOUND — nothing identified as dropped; product line expanding (planar → VIO) [T1 neg]

WHAT IT HAS MADE — dated, measured

- Transmon QPUs (A-Line/D-Line) with >100 µs T1, commercially shipped — undated vendor claims, page accessed 2026-09-03 [T1 page / T3 claims]
- Josephson junctions with post-fabrication targeting and trimming — fabricated capability, wafer-level frequency control implied [T1/T3]
- VIO 3D vertical interconnect shipping in planar / 176-line form; larger variants are roadmap only [T1/T3]

Open *Does QuantWare run its own fab line or fabricate elsewhere (e.g., TU Delft Kavli Nanolab)? Load-bearing for classification — do not assert owner-operator · Al or Nb? 'Negligible kinetic inductance' hints at Al or thick Nb; has any customer's own design actually run through Foundry Services since 2022? · Is VIO-400 (slated 2026) shipping? No confirmation found; is QuantWare SUPREME's unnamed Dutch fab site (TNO/Delft, Single Quantum also candidates)?*

Profile compiled from public sources and dated to 2025-07; tiers as marked; NOT FOUND = searched and not found. One of fourteen fab profiles; the matrix on p. 15 is their summary. Full references: p. 17.

Changed since v1.0 — what a reader of the August edition should re-read

CORRECTED — v1.0 printed → v1.1 prints

• **"No commercial EDA flow"; EDA SRL 2–3 →** the physical-verification layer is a commercial product line from one supplier (SRL 5); above RTL nothing is licensable (SRL 4). Memory, not EDA, is the lowest gating subsystem (SRL 3).

• **Venture ~$110M; SEEQC $52.4M →** ≈$140M; SEEQC $80.8M gross per SEC filings.

• **IonQ–SkyWater "$15 cash + $20 stock, $35.00" →** $15.00 cash + 0.4883 IonQ shares per share.

• **D-Wave "1,030,000-JJ chips" →** "more than a million JJ" — the vendor's statement; the exact figure has no primary.

• **Per-qubit control ratio "~10^6×" →** a span from ~40× to ~10^7×, and the two figures are budgeted at different fridge stages (p. 11).

• **imec "six ASC 2026 talks" →** fourteen entries with imec authors, eleven imec-led — still no measured logic gate.

• **"Readout blocks already ~20 µW" →** the anchor is a spin-qubit charge-readout IC (18.5 µW/qubit, ISSCC 2025), a different modality.

• **"AIST CRAVITY" →** AIST QuFab (renamed 2024); the HSTP node its one foreign customer used is off the FY2026 menu.

NEW SINCE THE 9 AUGUST CUT-OFF

• **SEEQC:** Allegro SPAC terminated 25 Aug 2026; the S-1 filed 29 Jun was amended 28 Aug (p. 8, p. 16).

• **SkyWater:** SEC reporting ended — Form 15 filed 10 Aug 2026; the FTC was equally divided on the acquisition, so its behavioural order failed of adoption (p. 8).

• **mK SFQ control:** a third independent party, NICT + Tohoku (EPJ QT, 9 Jul 2026) — published before the August cut-off and missed by it; a probable fourth in Shenzhen (p. 4, p. 16).

• **Market anchors:** WSTS Spring-2026 forecast entered — $1.51T in 2026, ~$1.9T in 2027 (p. 9).

• **Capacity builds:** Anderon (IBM + Commerce, May 2026) and SUPREME (Chips JU) entered — both qubit-aimed, neither names a flux-logic family (p. 8, p. 16).

• **Data cut-off:** 6 September 2026, single and clean; the market model was re-verified anchor by anchor on 5 September and found current.

STRUCTURE, SCORING, NAME

• **Renamed** Superconductor Electronics Monitor — the field's own umbrella; SFQ is its largest branch (p. 2). The all-versions DOI is unchanged.

• **New pages:** the family taxonomy (p. 5), density — the ceiling, the levers and who holds them (p. 13), who makes what (p. 15), fourteen fab profiles (pp. 18–31), and this page.

• **SRL re-scored:** QC control 6, the field's highest; EDA split physical 5 / system 4; memory 3. Everything else unchanged.

• **Reclassified:** the 809k-JJ chip is the largest all-junction memory ever built (202,280 bits), filed in v1.0 under logic only; nine fabs, one contested, have made SCE logic — v1.0's "five of fifteen lines" counted roadmap-table organisations.

• **Left open, printed as such:** which award maintains qPALACE today; whether NEC's process runs in its own facility; whether the Shenzhen flux-DAC work counts as a fourth control party.

Not changed: every scenario band, every scenario weight and every absolute market figure. v1.0 (9 Aug 2026) remains citable as v1.0 at doi:10.5281/zenodo.21860768; this edition is doi:10.5281/zenodo.22537315; the all-versions link doi:10.5281/zenodo.21860767 always resolves to the current edition.

Corrections are listed against the printed wording of v1.0; Full references: p. 17.

Superconductor Electronics Monitor 2026

v1.1 · data cut-off 6 September 2026 · released September 2026

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