SFQ Technology Monitor 2026

Single Flux Quantum superconducting digital electronics — markets, money, maturity.

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About this report

What you will find in this Monitor

A market and technology view of superconducting SFQ (Single Flux Quantum) digital electronics: where money is being made and invested today, how the contestable market develops to 2035, and the technological maturity that gates it. Every figure carries a source, a date, and a confidence tier.

HOW TO READ THE NUMBERS

T1	Demonstrated — primary peer-reviewed / datasheet source
T2	Corroborated — multiple independents tracing to a primary
T3	Vendor claim — single-source, not reproduced
T4	Modeled estimate — our scenario; assumptions stated

SECTIONS

Every figure on these slides carries its confidence tier; sources are cited per slide and compiled, grouped, in the References (p. 14).

The primer

What is SFQ? Superconducting digital electronics built from Josephson junctions — the fastest, lowest-energy logic ever demonstrated

T1

$\Phi_0 = h/2e$

the bit itself: one magnetic flux quantum = 2.067 833 848 × 10^{-15} Wb — a constant of nature, identical in every device, immune to drift

T1

~1 ps

Josephson-junction switching — logic demonstrated to 770 GHz (1999), still the fastest digital gate ever clocked in any technology

T1/T4

~10^{-19} J

energy per switch (ERSFQ) — ~1,000× below CMOS before the cryogenic tax, a conditional 10–30× after it

The Landauer frontier: adiabatic AQFP is measured at ~35× kT·ln2 at GHz speeds (a 21,460-JJ CPU exists); sub-Landauer switching remains reversible-and-simulated only — it costs ~10^3× in density and pays off first in qubit control, not CPUs. [T1 device / T4 system]

HOW IT COMPUTES

- Bits are single quanta of magnetic flux stored in superconducting loops; Josephson junctions switch in ~1 ps, emitting identical picosecond pulses instead of holding voltage levels
- Zero-resistance wiring carries those pulses ballistically — interconnect energy, the dominant cost in CMOS, nearly vanishes
- Circuits run at 4 kelvin in niobium foundry processes at 150–350 nm — 1990s-scale lithography at an exotic operating point
- One family, several dialects — RSFQ (1991) · ERSFQ/eSFQ · RQL · AQFP — this Monitor covers them all as "SFQ"

WHAT IT IS NOT (the honest limits)

- Not dense: ~10^3–10^4× behind CMOS per mm²; the largest 4 K RAM ever demonstrated is 64 kb (2013) — memory is the field's hardest gate
- Not room-temperature: every watt removed at 4.2 K costs ~230–7,000 W at the wall — the cryogenic tax, priced into every figure here
- Not mainstream: a handful of foundries, no commercial EDA flow — ecosystem, not physics, sets today's pace

Sources: Chen & Likharev 1999 (770 GHz) · Mukhanov 2011 (ERSFQ) · Cryomech PT415 (cryogenic tax) / plant-FOM data. *Full references: p. 14.*

The highest speed, the asymptotically lowest energy, and the symbiosis with quantum computing secure a growing long-term future for SFQ

CONTROLLING QUANTUM COMPUTERS

The near market driven by QC

- Superconducting-qubit machines hit a wiring wall: room-temperature control tops out near ~10^3 lines per cryostat — 10^5–10^6-qubit machines need electronics inside the fridge (Google control team, 2019; ETH budget analysis, 2019)
- SFQ is the only logic family that has demonstrated qubit-control waveform synthesis at millikelvin — up to 99.9% single-qubit fidelity (two-chip stack, Nature Electronics 2026)
- IBM is exploring SFQ control with SEEQC under DARPA's QBI (2025); Japan's Moonshot funds SFQ qubit control & readout as a named theme

Contested by cryo-CMOS at 3–4 K (2–23 mW/qubit demonstrated) — this Monitor tracks both.

ENERGY-FRONTIER COMPUTING

The large, distant prize

- Projected 0.025 J/TFLOP wall-plug for a superconducting AI system incl. cooling — ~18× below Blackwell-class like-for-like (imec; projection, not silicon)
- Gated by memory (the 64 kb record) and by finding an accelerator model that fits SFQ's strengths

The bull case lives or dies here — see Market development (p. 8).

THz-CLASS ELECTRONICS

The top-speed edge

- Holds the outright digital speed record — a 770 GHz SFQ flip-flop (1999), unbeaten in any technology; complex circuits run at upper tens of GHz today (junction limit ~1 THz, fc ≈ 870 GHz)
- Fielded for over a decade in defense digital-RF receivers; a natural readout for superconducting single-photon-detector arrays

Small markets today — but the capability is unique and shipping.

Sources: Krinner et al., EPJ QT (2019); Bardin et al., JSSC (2019); Underwood et al., PRX Quantum (2024); SEEQC, Nature Electronics (2026); DARPA QBI (Jun 2025); JST Moonshot Goal 6; imec (2024). Full references: p. 14.

Key takeaways

Small money today, a defined path to billions — gated by physics we can name

T4

$4–9B

probability-weighted contestable market, 2035 (computed $4.3–8.8B; bear $0.5–1.5B · base $3–8B · bull $20–35B)

T2

~$110M

total disclosed funding into SFQ-first startups to date — vs $12.6B into quantum startups in 2025 alone: early, tiny, pre-inflection

T1

$1.8B

IonQ's completed acquisition of SkyWater (closed 31 Jul 2026) — the first SFQ-capable fab now inside a quantum vendor

T4

$0.1–0.3B

today’s SFQ-linked annual revenue base: defense digital-RF, metrology, QC-control co-development

770 GHz

fastest digital logic ever demonstrated — RSFQ, 1999

64 kb

the 4 K RAM record, unbeaten since 2013 — memory gates general-purpose SFQ

×230–7,000

the cryogenic tax: ~1000× raw energy edge becomes a conditional 10–30×

~nW/qubit

projected ERSFQ control vs 2–23 mW/qubit demonstrated cryo-CMOS — why revenue starts in quantum

Sources: Chen & Likharev (1999); Van Duzer et al. (2013); cryogenics per Cryomech/NIST specs; Bardin (2019) & Underwood (2024); company filings & disclosures; McKinsey QTM 2026 (context); T4 = Qodeh scenarios, assumptions stated (p. 8). Full references: p. 14.

Where SFQ earns money today: three lines — two of them quantum computing

GATE-MODEL QC: CONTROL & READOUT

The physics-favored segment

- SEEQC: only shipping mK-SFQ control hardware — QC controlled by SFQ digital electronics at millikelvin (Nature Electronics, 2026)
- NVIDIA NVQLink QPU–GPU digital link (2025); digital QEC interface with UK NQCC (2025)
- Customer-funded co-development: BASF, Merck lineage (QuPharma)

CO-DEVELOPMENT → EARLY PRODUCT

DEFENSE DIGITAL-RF

The quiet installed base

- Superconductor direct-RF receivers fielded for over a decade (Hypres lineage): 20–30 GHz sampling ADCs, ~75 dB SINAD class
- Renewed ADC demonstrations published 2025
- Opaque, defense-funded; ~low hundreds of $M with metrology & SQUIDs combined

NICHE PRODUCT (SUSTAINED)

ANNEALING QC: DACs AT SCALE

Also quantum computing — and the manufacturability proof

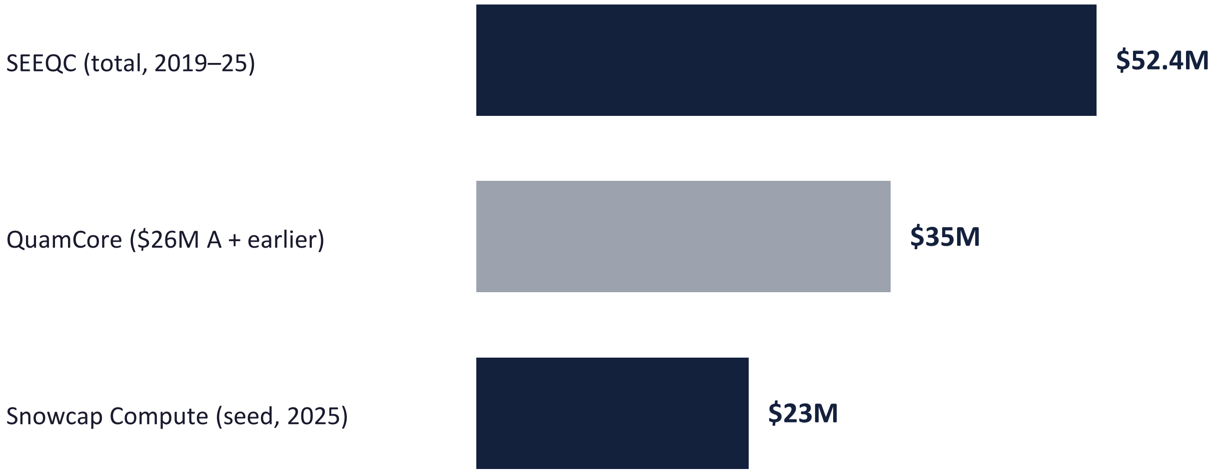
- Annealing is QC: D-Wave ships 1,030,000-JJ chips since 2020 — on-chip SFQ/QFP DACs program every annealer
- The largest superconducting ICs in production anywhere
- Proves 10^6-JJ manufacturability the AI/HPC thesis depends on

IN PRODUCTION (ADJACENT)

Full references: p. 14.

SFQ-first venture layer

Disclosed equity into SFQ-first companies, $M — an upper bound on SFQ-directed venture money



Three ledgers, read differently: (1) Venture — ~$110M cumulative into SFQ-first companies: an upper bound on SFQ-directed money (these companies also fund qubits, foundry services, and full systems; pure-play floor: Snowcap's $23M); ≈0.4% of 2025 quantum equity. (2) Corporate/M&A — the $1.8B SkyWater acquisition moved the only SFQ production fab inside a quantum vendor; the SFQ-attributable share of the price is not derivable. (3) State, the majority — mostly undisclosed; disclosed anchors: CAS RMB 1B (~$145M) initiative, NSF DISCoVER $15.0M Expedition, a DOE Accelerate share; order $150–400M/yr [T4]. The venture ledger — three disclosed companies worldwide — is the smallest and the most information-rich: its near-emptiness is itself evidence, and inflections announce themselves there first.

THE STRUCTURAL EVENT

$1.8B

IonQ → SkyWater ($15 cash + $20 IonQ stock per share, $35.00): announced Jan 2026, shareholder-approved May 2026, closed 31 Jul 2026 — SkyWater operates as a subsidiary under its own name, with a general foundry-continuity pledge and Category-1A Trusted Foundry status retained. The first SFQ-capable Trusted Foundry now inside a vertically integrated quantum vendor — superconducting-program-specific continuity (e.g., the QuamCore co-development) remains the open question. The SFQ-attributable share of the price is not derivable: SkyWater does not disclose its SFQ revenue.

New (Jun–Jul 2026): SEEQC filed an S-1 toward a Nasdaq listing (Jun 29), parallel to its Jan-2026 Allegro SPAC path at a reported ~$1B valuation — the first SFQ pure-play approaching public markets [T2]. **Program signal:** still no dedicated US superconducting-digital program since IARPA C3.

Sources: TechCrunch (Jan 2025); BusinessWire (Jun 2025); Ctech (Aug 2025, T2) + inferred pre-A (T3); IonQ/SkyWater filings; CAS: China Daily (2018); NSF award #2124453; McKinsey QTM 2026. *Full references: p. 14.*

Market development

Three market-size scenarios to 2035

BEAR

~50% probability

$0.5–1.5B

Memory stays unsolved; imec-class milestones slip; QC scaling slips. SFQ = QC control + defense RF niche.

BASE

~35% probability

$3–8B

QC control scales with 10^5-qubit machines; first cryo-AI inference pods deployed ~2030–32.

BULL

~15% probability

$20–35B

Rack-level 10–30× J/FLOP proven ~2030; energy-constrained AI buildout adopts cryo-pods (3–5% of accelerators).

Scenario-weighted mean ≈ $6.5B (endpoint band $4.3–8.8B): the mode is bear, yet the mean lands in upper-base — ~2/3 of it rides the 15% bull branch. Anchors — four different denominators: semiconductors $796B, 2025 (WSTS) · AI accelerators $373B by 2030 → >$600B by 2033 (system-level; not a WSTS subset) · QC $43–71B by 2035 (all modalities; SFQ rides the superconducting share) · datacenter electricity 945 TWh/yr (~0.95 PWh) by 2030. SFQ contests value in fixed-infrastructure markets, never volume.

Source: Qodeh scenarios (T4, drivers stated); WSTS 2025; MarketsandMarkets 2025; McKinsey QTM 2026; IEA, Energy & AI 2025. A cryostat excludes mobile/client/edge — ~75% of logic demand. *Full references: p. 14.*

Four markets: when each turns on and what gates it

QC control & the QC→HPC interface

$0.5–2B by early 2030s

Physics-favored: the only logic demonstrated synthesizing control at mK; cryo-CMOS contests at 3–4 K (2–23 mW/qubit). Revenue exists now; scales with every 10^5-qubit program.

Gate: qubit-count scale-up itself

AI / HPC acceleration

$0 – $35B by 2035

Entirely scenario-dependent: wall-plug J/FLOP edge is ~18× on paper (BF16 vs B200), unproven in silicon.

Gates in order: memory (binary unlock) → system proof → miniaturization & 3D (throttle: sets whether share is 1% or 5%)

Defense digital-RF

$0.3–1B

Fielded niche with decades of heritage; grows with SIGINT/radar modernization; opaque budgets.

Gate: program-of-record wins

Metrology & other

~$0.1B

Josephson voltage standards, SQUID-adjacent; mature, stable, small.

Gate: none — steady state

Source: Qodeh scenario decomposition (all T4); gate evidence per *References (p. 14)**. QC-control estimate = share of QC systems capex crossing to in-fridge digital control.*

Three numbers carry the whole thesis

×10

system clock vs CMOS (40–60 GHz vs 5–6 GHz) — device physics allows ×100 more

Engineering, not physics, is the current limiter

10–30×

conditional net energy edge after the ×230–7,000 cryogenic tax — from zero leakage, near-zero interconnect energy, 3D stacking

Only a built system can prove it; none has

~10^6×

ERSFQ's projected per-qubit power edge over cryo-CMOS control at mK — the stage where no other logic family has demonstrated waveform synthesis

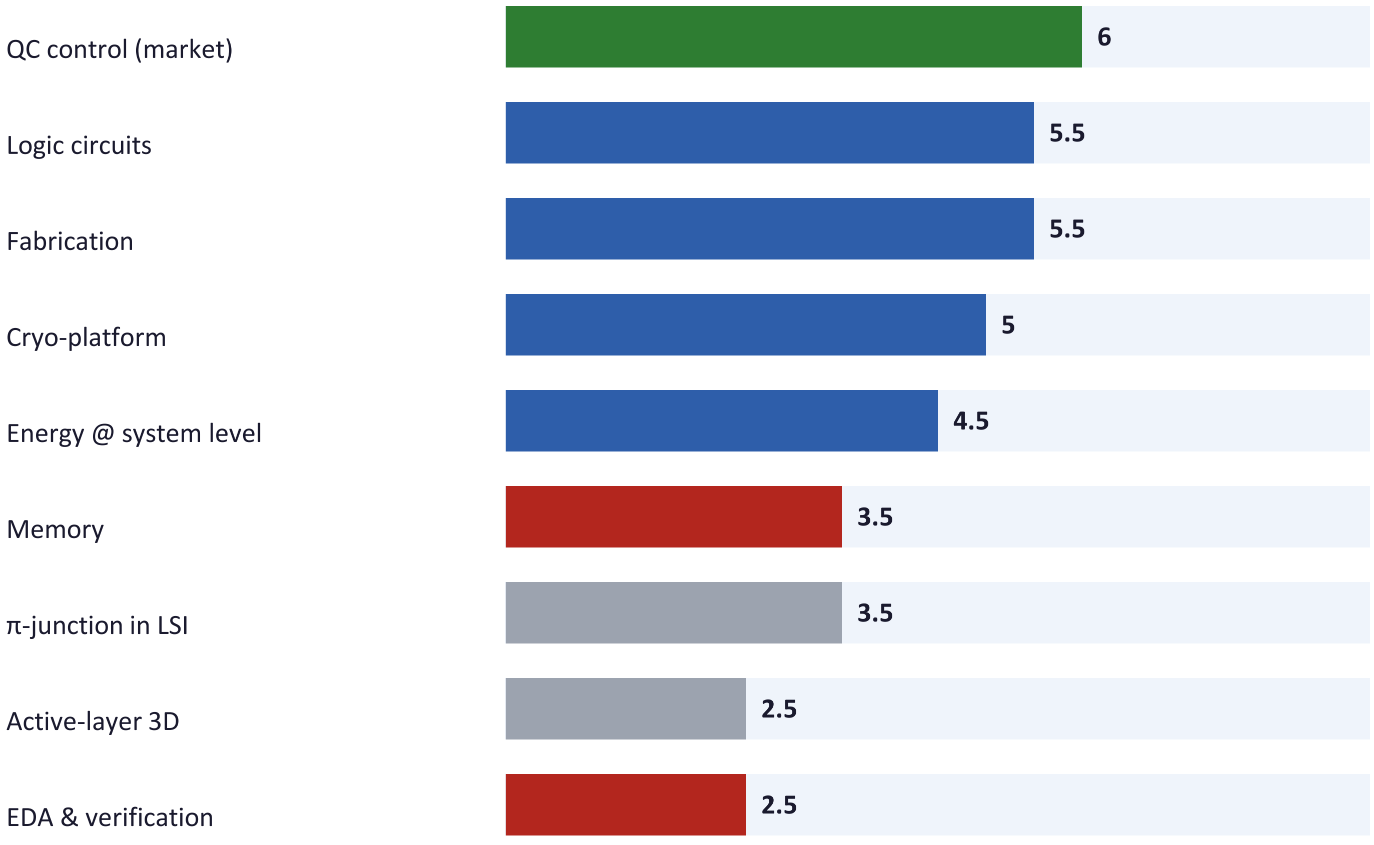
This is why revenue starts in quantum, not AI

Every figure above carries its tier and re-derives from physical constants and published specifications — the Monitor's core discipline.

Sources: NVIDIA H100 / B200 datasheets; Cryomech / plant specifications; Herr et al. (2011, 2013); McDermott et al. (2018). *Full references: p. 14.*

Readiness is wildly uneven — and the two lowest bars gate the biggest money

SFQ-Readiness Level (SRL, 1–9) by subsystem — never blended



THE TWO GATES

Memory (SRL 3–4). 4 K RAM record: 64 kb, 2013. Every dense new line is sub-4 K, destructive, simulation-only, or unfabricated. The AI thesis rests on an unbuilt part (imec JSRAM).

EDA & verification (SRL 2–3). No commercial flow; timing is function; test can't probe 4 K at speed. The field's largest unowned niche.

SRL = SFQ-Readiness Level: a TRL-analogous 1–9 judgment per subsystem, assigned by Qodeh from the demonstrations referenced on p. 14 — the scale is a judgment, the basis is T1.

Players by layer

FABS & PLATFORMS

- MIT Lincoln Lab — SFQ5ee/SC1/SC2, the research standard
- imec — 300-mm CMOS-compatible NbTiN platform (IEDM 2024)
- SEEQC foundry (ex-Hypres) · AIST CRAVITY · SIMIT (CN)
- SkyWater — Trusted Foundry; IonQ subsidiary since 31 Jul 2026
- FLUXONICS (Leibniz IPHT Jena) — European MPW, RSFQ1 rules

PRODUCT & VENTURE

- SEEQC — mK-SFQ control; $52.4M raised; NVIDIA/NVQLink
- Snowcap Compute — SFQ-for-AI; $23M seed (Jun 2025)
- QuamCore — monolithic mK architecture; $35M reported
- D-Wave — 10^6-JJ chips in production · Hypres — digital-RF
- Northrop Grumman — RQL (publicly quiet 2024–26)

PROGRAMS & RESEARCH

- No US superconducting-digital program since IARPA C3
- Japan: ¥130B quantum supplement (2025); AIST ¥100B
- Yokohama/Nagoya — AQFP, ALUs, π-junctions
- Rochester (Friedman) — design canon · MIT — nanowire memory
- Wisconsin/NIST — SFQ qubit control · USC — EDA/architecture

Source: company/press disclosures 2024–26 (References, p. 14; T1–T3 by item). Fab and company columns: complete as publicly disclosed at cut-off; research poles: selected. Names are public facts, not endorsements.

The events that move the scenario weights

WOULD MOVE THE NUMBERS UP

- imec's first 300-mm logic silicon — IEDM 2025 delivered process advances only (JJ density, flux-trap mitigation); the six ASC 2026 talks are fabrication/platform + an invited multiphase-AC power study, no logic claim; watch IEDM 2026/27
- A fabricated JSRAM macro — validates the entire SFQ-AI roadmap
- Any 4 K RAM beyond 64 kb — resets a 13-year record
- Snowcap tapeout or architecture disclosure
- SEEQC listing terms (S-1/SPAC) — first public SFQ pure-play
- A new major government/defense superconducting-digital program — US, EU, Japan, or allied
- π-junction phase-battery circuits at $\geq 10^3$ JJ on foundry Nb — a cell-size lever for RSFQ and AQFP alike

WOULD MOVE THE NUMBERS DOWN

- IonQ–SkyWater integration: general continuity pledged at close (31 Jul 2026) — watch superconducting-specific commitments (QuamCore co-development)
- imec platform slip — metric: no $\geq 10^3$-JJ clocked logic on 300 mm and no fabricated JSRAM array by end-2027
- Cryo-CMOS full control at ≤10 µW/qubit — the 4 K-budget line at 10^5 qubits; readout blocks already ~20 µW
- A quantum funding winter — freezes the QC-control bridge; defense RF becomes the floor
- Flux-trapping or yield surprises at $>10^6$ JJ integration

Items map to the scenario drivers (p. 8), the market gates (p. 9), or the funding ledgers (p. 7). Watch venues: ASC 2026 (Sep 6–11, Pittsburgh) — imec's six talks · IEDM 2026/27 (San Francisco) · ISS (Japan, annual).

Published sources behind this Monitor

PEER-REVIEWED LITERATURE & PREPRINTS

Foundations & records: Likharev & Semenov, IEEE TAS 1 (1991) · Chen et al., IEEE TAS 9 (1999) · Mukhanov, IEEE TAS 21 (2011) · Herr et al., JAP 109 (2011) · Herr et al., JAP 113 (2013) · Takeuchi et al., APL 102 (2013) · APL 114 (2019) · Sci. Rep. 4 (2014) · Sci. Rep. 7 (2017) · npj QI 10 (2024) · Ayala et al., IEEE JSSC 56 (2021) · Van Duzer et al., IEEE TASC 23 (2013)

Fabrication & scaling: Tolpygo et al., IEEE TAS 25 (2015) · IEEE TAS 29 (2019) · Golden et al., arXiv:2501.03343 (2025) · Tolpygo et al., arXiv:2411.04045 (2024) · imec: IEDM 2024 · IEDM 2025 · IITC 2026 · Kundu et al. (imec), arXiv:2411.08645 (2024) · Herr et al., APL 122 (2023) · Medeiros et al., Nature Electronics 9 (2026) · Krylov, Jabbari & Friedman, Springer (2024)

Quantum control & decode: Krinner et al., EPJ QT 6:2 (2019) · Bardin et al., IEEE JSSC 54 (2019) · Underwood et al., PRX Quantum 5 (2024) · Acharya et al., Nature Electronics 6 (2023) · McDermott & Vavilov, PR Applied 2 (2014) · McDermott et al., QST 3 (2018) · Leonard et al., PR Applied 11 (2019) · Liu et al., PRX Quantum 4 (2023) · SEEQC et al., Nature Electronics 9 (2026) · Google Quantum AI, Nature 638 (2025) · Ueno et al., DAC (2021) · HPCA (2022) · Holmes et al., ISCA (2020)

DATASHEETS & TECHNICAL SPECIFICATIONS

NVIDIA H100 · NVIDIA B200 / Blackwell · Cryomech PT415 (Bluefors) · Bluefors XLD/XLDsl · Oxford Instruments Proteox · MIT Lincoln Laboratory foundry · FLUXONICS RSFQ1H rules · CMOS node data (ISSCC 2025 / IEEE Spectrum)

COMPANY FILINGS & DISCLOSURES

D-Wave (QBTS) 10-K FY2025 · SkyWater (SKYT) 10-K FY2025 · IonQ–SkyWater close (31 Jul 2026) · SEEQC S-1 (Jun 2026) · SEEQC $30M (TechCrunch, Jan 2025) · SEEQC Series A (BusinessWire, 2020) · Snowcap Compute launch (Jun 2025) · QuamCore Series A (Ctech, Aug 2025) · NVIDIA NVQLink (Oct 2025) · SkyWater–QuamCore (Nov 2025) · D-Wave Advantage2 GA (May 2025)

GOVERNMENT & PROGRAM DOCUMENTS

IARPA C3 · IARPA SuperTools · DARPA QBI — IBM × SEEQC (Jun 2025) · JST Moonshot Goal 6 · US DOE “Accelerate” (Sep 2023) · NSA Superconducting Technology Assessment (2005) · EU Chips-JU / NanoIC (2026)

MARKET CONTEXT

McKinsey Quantum Technology Monitor (2026) · WSTS (2025) · MarketsandMarkets accelerator forecast (2025) · IEA, Energy & AI (2025) · Europractice MPW prices (2026)

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Underlying Qodeh research analyses are available on request.

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